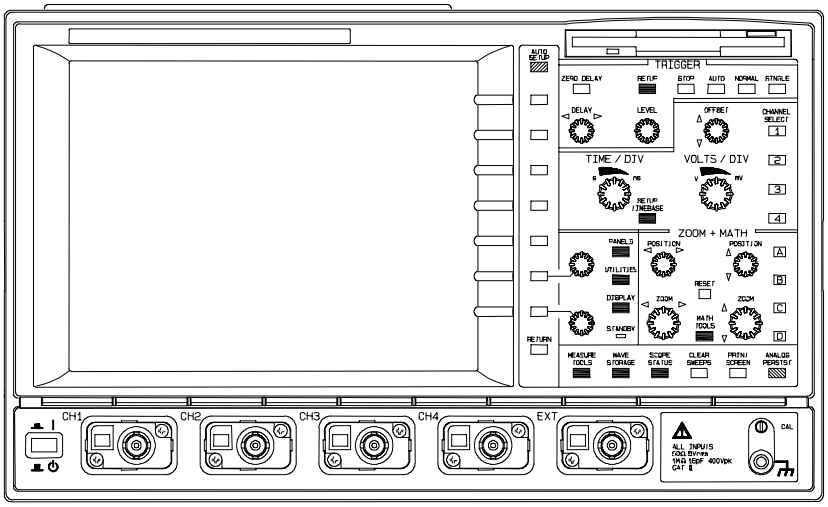
LeCroy Waverunner2 Series

Service Manual



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LeCroy

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LeCroy

1. Warranty and Product Support

It is recommended that you thoroughly inspect the contents of the oscilloscope packaging immediately upon receipt. Check all contents against the packing list/invoice copy shipped with the instrument. Unless LeCroy is notified promptly of any missing or damaged item, responsibility for its replacement cannot be accepted. Contact your nearest LeCroy Customer Service Center or national distributor immediately (see chapter 2 for *contact numbers*).

1.1 Warranty

LeCroy warrants its oscilloscope products for normal use and operation within specifications for a period of three years from the date of shipment. Calibration each year is recommended to ensure in-spec. performance. Spares, replacement parts and repairs are warranted for 90 days. The instrument's firmware has been thoroughly tested and is thought to be functional, but is supplied without warranty of any kind covering detailed performance. Products not made by LeCroy are covered solely by the warranty of the original equipment manufacturer.

Under the LeCroy warranty, LeCroy will repair or, at its option, replace any product returned within the warranty period to a LeCroy authorized service center. However, this will be done only if the product is determined after examination by LeCroy to be defective due to workmanship or materials, and not to have been caused by misuse, neglect or accident, or by abnormal conditions or operation.

1.2 Product Assistance

Note: This warranty replaces all other warranties, expressed or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract or otherwise. The client will be responsible for the transportation and insurance charges for the return of products to the service facility. LeCroy will return all products under warranty with transport prepaid.

Help on installation, calibration, and the use of LeCroy equipment is available from the LeCroy Customer Service Center in your country.

1.3 Maintenance Agreements

LeCroy provides a variety of customer support services under Maintenance Agreements. Such agreements give extended warranty and allow clients to budget maintenance costs after the initial three-year warranty has expired. Other services such as installation, training, enhancements and on-site repairs are available through special supplemental support agreements.

1.4 Staying Up to Date

LeCroy is dedicated to offering state-of-the-art instruments, by continually refining and improving the performance of LeCroy products. Because of the speed with which physical modifications may be implemented, this manual and related documentation may not agree in every detail with the products they describe. For example, there might be small discrepancies in the values of components affecting pulse shape,

timing or offset, and — infrequently — minor logic changes. However, be assured the scope itself is in full order and incorporates the most up-to-date circuitry. LeCroy frequently updates firmware and software during servicing to improve scope performance, free of charge during warranty. You will be kept informed of such changes, through new or revised manuals and other publications.

Nevertheless, you should retain this, the original manual, for future reference to your scope's unchanged hardware specifications.

1.5 Service and Repair

Please return products requiring maintenance to the Customer Service Department in your country or to an authorized service facility. The customer is responsible for transportation charges to the factory, whereas all in-warranty products will be returned to you with transportation prepaid. Outside the warranty period, you will need to provide us with a purchase order number before we can repair your LeCroy product. You will be billed for parts and labor related to the repair work, and for shipping.

1.6 How to return a Product

Contact the nearest LeCroy Service Center or office to find out where to return the product. All returned products should be identified by model and serial number. You should describe the defect or failure, and provide your name and contact number. In the case of a product returned to the factory, a Return Authorization Number (RAN) should be used.

Return shipments should be made prepaid. We cannot accept COD (Cash On Delivery) or Collect Return shipments. We recommend air-freighting.

It is important that the RAN be clearly shown on the outside of the shipping package for prompt redirection to the appropriate LeCroy department.

1.7 What Comes with Your Scope

The following items are shipped together with the standard configuration of this oscilloscope:

- Front Scope Cover
- 10:1 10 MΩ PP006 Passive Probe — *one per channel*
- *Two* 6.3A 250 V Fuses, AC Power Cord and Plug
- *Operator's Manual* , *Remote Control Manual, Hands-On Guide*
- Performance Certificate or Calibration Certificate, Declaration of Conformity

Note: Wherever possible, please use the original shipping carton. If a substitute carton is used, it should be rigid and packed so that that the product is surrounded by a minimum of four inches or 10 cm of shock-absorbent material.

2. General Information

2.1 Product Assistance

Help on installation, calibration, and the use of LeCroy equipment is available from your local LeCroy office, or from LeCroy's

- Customer Care Center, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977–6499, U.S.A., tel. (845) 578–6020
- European Service Center, 4, Rue Moïse Marcinhes, 1217 Meyrin 1, Geneva Switzerland, tel. (41) 22/719 21 11.
- LeCroy Japan Corporation, Sasazuka Center Bldg – 6th floor, 1-6, 2-Chome, Sasazuka, Shibuya-ku, Tokyo Japan 151-0073, tel. (81) 3 3376 9400

2.2 Installation for Safe and Efficient Operation

Operating Environment

For safe operation of the instrument to its specifications, ensure that the operating environment is maintained within the following parameters:

Temperature ..... 5 to 40 °C (41 to 104 °F) rated.

Humidity ..... Maximum relative humidity 80 % RH (non-condensing) for temperatures up to 31 °C decreasing linearly to 50 % relative humidity at 40 °C

Altitude ..... < 2000 m (6560 ft)

The oscilloscope has been qualified to the following EN61010-1 category:

Installation (Overvoltage) Category II

Protection Class ..... … I

Pollution Degree 2

Safety Symbols

Where the following symbols or indications appear on the instrument's front or rear panels, or elsewhere in this manual, they alert the user to an aspect of safety.


..... **CAUTION**: Refer to accompanying documents (for Safety-related information). *See elsewhere in this manual wherever the symbol is present.*

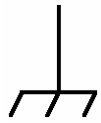

..... **CAUTION**: Risk of electric shock


..... **On (Supply)**

..... Standby **(Supply)**


..... **Earth (Ground) Terminal**


..... **Alternating Current Only**


..... **Chassis Terminal**


..... **Earth (Ground) Terminal on BNC Connectors**

WARNING..... **Denotes a hazard. If a WARNING is indicated on the instrument do not proceed until its conditions are understood and met.**


WARNING

Any use of this instrument in a manner not specified by the manufacturer may impair the instrument's safety protection.

The oscilloscope has *not* been designed to make direct measurements on the human body. Users who connect a LeCroy oscilloscope directly to a person do so at their own risk. Use only indoors.

Power Requirements

The oscilloscope operates from 90–132 V AC 45-440 Hz, and 180–250 V AC; 45–66 Hz. No voltage selection is required, since the instrument automatically adapts to the line voltage present.

Fuses

The power supply of the oscilloscope is protected against short-circuit and overload by means of two **6.3 A/250 V AC** "T"-rated fuses, located above the mains plug.

Disconnect the power cord before inspecting or replacing a fuse. Open the fuse box by inserting a small screwdriver under the plastic cover and prying it open. For continued fire protection at all line voltages, replace only with fuses of the specified type and rating (*see above).*

Ground

The oscilloscope has been designed to operate from a single-phase power source, with one of the current-carrying conductors (neutral conductor) at ground (earth) potential. Maintain the ground line to avoid an electric shock.

None of the current-carrying conductors may exceed 250 V rms with respect to ground potential. The oscilloscope is provided with a three-wire electrical cord containing a three-terminal polarized plug for mains voltage and safety ground connection. The plug's ground terminal is connected directly to the frame of the unit. For adequate protection against electrical hazard, this plug must be inserted into a mating outlet containing a safety ground contact.

Cleaning and Maintenance

Maintenance and repairs should be carried out exclusively by a LeCroy technician. Cleaning should be limited to the exterior of the instrument only, using a damp, soft cloth. Do not use chemicals or abrasive elements. Under no circumstances should moisture be allowed to penetrate the disk drive analyzer. To avoid electric shocks, disconnect the instrument from the power supply before cleaning.

CAUTION

Risk of electrical shock: No user-serviceable parts inside. Leave repair to qualified personnel.

Power On

Connect the oscilloscope to the power outlet and switch it on using the power On/Standby button, located near the left-hand corner of the instrument below the screen. After the instrument is switched on, auto-calibration is performed and a test of the disk drive analyzer's ADCs and memories is carried out. The full testing procedure takes approximately 10 seconds, after which time a display will appear on the screen.

3 Specifications

3.1 Models

Waverunner2 LT372/262 Series: Two channels

Waverunner2 LT584/374/354/264 Series: Four channels

3.2 Vertical System

Bandwidth (–3dB): LT584: 1 Ghz; **LT374/372/354:**500 MHz; **LT264/262**:350 MHz @ 50 Ω

Bandwidth Limiter: 20 MHz and 200 MHz can be selected for each channel.

Input Impedance: 50 Ω ± 1.0 %; 1 MΩ ± 1.0 % // 12 pF typical using PP006 probe

Input Coupling: 1 MΩ: AC, DC, GND; 50 Ω: DC, GND

Max Input: 50 Ω: 5 Vrms; 1 MΩ: 400 V max (peak AC <-5 kHz + DC)

Vertical Resolution: 8 bits; up to 11 bits with enhanced resolution (ERES)

Sensitivity (50 Ω or 1 MΩ): 2 mv - 10V/div fully variable

Offset Range:

- 2 mV–99 mV/div: ± 1 V
- 100 mV–0.99 mV/div: ± 10 V
- 1 V–10 V/div: ± 100 V

Isolation - Channel to channel: >250:1 at same V/div settings

3.3 Timebase System

Timebases: Main and up to four zoom traces simultaneously

Time/Div Range: LT374/372/LT584: 500 ps/div 1000 s/div, **LT264/262/354:** 1 ns/div to 1000 s/div

Clock Accuracy: ≤ 10 ppm

Interpolator Resolution: 5 ps

External Clock: ≤ 500 MHz, 50 Ω, or 1 MΩ impedance

Roll Mode: time/div 500 ms - 1000 s/div or sample rate <100 kS/s max

3.4 Acquisition System

Single Shot Sample Rate	LT584/M/L	LT374/M/L	LT372	LT264/M	LT262	LT354/M/ML
1 Channel Max	4 GS/s	4 GS/s	4 GS/s	1 GS/s	1 GS/s	1 GS/s
2 Channels Max	4 GS/s	4 GS/s	2 GS/s	1 GS/s	1 GS/s	1 GS/s
3-4 Channels Max	2 GS/s	2 GS/s	NA	1 GS/s	NA	1 GS/s
Maximum Acq Points/Ch						
1 Channel Max	500k/2M/8M	500k/2M/8M	500k	100k/1M	100k	500K/1M/2M
2 Channels Max	500k/2M/8M	500k/2M/8M	250k	100k/1M	100k	500K/1M/2M
3-4 Channels Max	250k/1M/4M	250k/1M/4M	NA	100k/1M	NA	250k/1M/4M

3.5 Acquisition Modes

Random Interleaved Sampling (RIS): 50 GS/s for repetitive signals 500 ps/div - 1 μs

Single Shot: For transient and repetitive signals: 1ns/div - 1000s/div

Sequence Mode:

LT262/264	2 - 400 segments
LT584/354/372/374	2 - 1000 segments
Memory Option M or L	2 - 400 segments
Intersegment Time	50 μsec max

3.6 Acquisition Processing

Averaging: Summed averaging to 10^3 sweeps; continuous averaging with weigthing range range from 1:1 to 1:1023 (standard). Summed averaging up to 10^6 sweeps (optional with WAVA)

Enhanced Resolution (ERES): From 8.5 to 11 bits vertical resolution

Envelope (Extrema): Envelope, floor, roof for up to 10^6 sweeps

3.7 Triggering System

Modes: NORMAL, AUTO, SINGLE and STOP

Sources: Any input channel, External, EXT 10 or line; slope, level and coupling are unique to each source (except line trigger). Inactive channels useable as trigger inputs.

Slope: Positive, Negative, Window

Coupling Modes: DC,AC,HFREJ,LFREJ

AC Cutoff Frequency	7.5 Hz typical
HFREJ, LFREJ	50 kHz typical
Pre-trigger delay	0 - 100% of horizontal time scale
Post-trigger delay	0 - 10000 divisions
Hold-off by time or events	Up to 20s or from 1 to 99,999,999 events
Internal trigger range	±5 div

Maximum Trigger Frequency: Up to 500 MHz (350 MHz on LT264/262)

External Trigger Input Range: ± 0.5 V, ± 5 V with Ext 10

Max external input @ 50Ω: ±5 V DC or 5Vrms

Max external input @ 1MΩ: 400 Vmax (DC + peak AC < 5 kHz)

3.8 Automatic Setup

Auto Setup: Automatically sets timebase, trigger, and sensitivity to display a wide range of repetitive signals.

Vertical Find: Automatically sets the vertical sensitivity and offset for the selected channels and display a waveform with maximum dynamic range.

3.9 Probes

Model PP006: PP006 with auto-detect: 10:1, 10 MΩ; one probe per channel

Probe System: ProBus Intelligent Probe System supports active, high-voltage, current, and differential probes, and differential amplifiers

Scale Factors: Up to 12 automatically or manually selected

3.10 Color Waveform Display

Type: VGA Color 8.4-inch flat-panel TFT-LCD

Resolution: 640 x 480 resolution

Screen Saver: Display blanks after 10 minutes (when screen saver is enabled)

Real Time Clock: Date, hours, minutes, and seconds displayed with waveform

Number of Traces: Display a maximum of eight traces. Simultaneously display channel, zoom, memory, and math traces

Grid Styles: Single, Dual, Quad, Octal, XY, Single+XY, Dual+XY; Full Screen gives enlarged view of each style

Intensity Controls: Separate intensity control for grids and waveforms

Waveform Styles: Sample dots joined or dots only — regular or bold sample point highlighting

Trace Overlap Display: Select opaque or transparent mode with automatic waveform overlap management

3.11 Analog Persistence Display

Analog Persistence and Color Graded Persistence: Variable saturation levels; stores each trace's persistence data in memory

Trace Selection: Activate Analog Persistence on a selected trace, top 2 traces, or all traces

Persistence Aging Time: Select from 500 ms to infinite

Trace Display: Opaque or transparent overlap

Sweeps Displayed: All accumulated or all accumulated with last trace highlighted.

3.12 Zoom Expansion Traces

Style: Display up to four zoom traces

Vertical Zoom: Up to 5x expansion, 50x with averaging

Horizontal Zoom: Expand to 2 pts/div, magnify to 50 000x

Autoscroll: Automatically scan and display any zoom or math trace

3.13 Rapid Signal Processing

Processor: Power PC

Processing Memory: Up to 128 Mbytes

Realtime Clock: Dates, hours, minutes, seconds, and time stamp trigger time to 1ns resolution.

3.14 Internal waveform Memory

Waveform: M1, M2, M3, M4; (Store full-length waveforms with 16 bits/data point)

Zoom and Math: Four traces A, B, C, D with chained trace capability

3.15 Setup Storage

For front panel and instrument status: Four non-volatile memories and floppy drive are standard; hard drive and memory card are optional

3.16 Interface

Remote Control: Full control of all front panel controls and internal functions via GPIB and RS-232-C, or Ethernet (optional)

GPIB Port: Full control via IEEE-488.2; configurable as talker/listener for computer control and data transfer

RS-232-C: Asynchronous transfer rate of up to 115.2 kbaud

Ethernet (optional): 10 Base-T Ethernet interface

Floppy Drive: Internal, DOS-format, 3.5" high-density

PC Card Slot (optional): Supports memory and hard drive cards

External Monitor Port Standard: 15-pin D-Type VGA-compatible

Centronics Port: Parallel printer interface

Internal graphics printer (optional): Provides hardcopy output in <10 seconds

3.17 Outputs

Calibrator signal: 500 Hz–1 MHz square wave or DC level, Select from –1.0 to +1.0 into 1MΩ, output on front panel test point and ground lug

Control signals: Rear panel, TTL level, BNC output, Choice of trigger ready, trigger out, or Pass/Fail status (output resistance 300 Ω ± 10 %)

3.18 Environmental and Safety

Operating Conditions: Temperature 5–40° C rated accuracy, 0-45°C operating, -20° - 60°C non-operating; humidity 80 % RH non-condensing up to 35° C, derates to 50% max RH, non-condensing at 45°C; 4500 m (15000ft) max up to 25°C; Derates to 2000 m (6600ft) at 45°C.

CE Approved: EMC Directive 89/336/EEC; EN61326-1 Emissions and immunity, Low Voltage Directive 73/23/EEC; EN 61010-1 Product Safety (Installation Category II, Pollution Degree 2)

UL and cUL: UL Standard UL 3111-1; cUL Standard CSA C22.2 No. 1010-1

3.19 General

Auto Calibration: Ensures specified DC and timing accuracy is maintained for 1 year minimum.

Auto Calibration Time: <500ms

Power Requirements: 90–132 V AC 45-440 Hz, and 180–250 V AC; 45–66 Hz; automatic AC voltage selection, maximum power dissipation 150 VA–230 VA, depending on model

Battery Backup: Front panel settings retained for two years minimum

Warranty and Calibration: Three years; calibration recommended yearly

3.20 Physical Dimensions

Dimensions (HWD): 210 mm x 350 mm x 300 mm (8.3" x 13.8" x 11.8"); height excludes scope feet

Weight: 8 kg (18 lbs.)

Shipping Weight: 12kg (27 lbs.)

3.21 Math Tools (Standard)

Simultaneously perform up to four math (signal) processing functions; traces can be chained together to perform math-on-math.

average (summed to 4000 sweeps)
Average (continuous weighted)
difference
enhanced resolution (to 11 bits)
envelope
FFT of 50 kpoint waveforms
floor
identity
negate
product
ratio
reciprocal (invert)
resample (deskew)
rescale (with units)
roof
sin x/x
sum

3.22 Measure Tools (Standard)

Automated measurements; Display any five parameters together with their average, high, low, and standard deviations.

amplitude	fall 90-10%	period
area	fall 80-20%	Phase
base	frequency	rise 10-90%
cycle mean	maximum	rise 20-80%
cycle rms	mean	rms
cycles	minimum	sdev
delay	+overshoot	top
∆delay	–overshoot	width
duty cycle	peak-to-peak	xamn
		xamx

3.23 Pass/Fail

Test any five parameters against selectable thresholds. Limit testing is performed using masks created on the scope or PC. Set up a pass or fail condition to initiate actions such as hard-copy output, saving waveform to memory, GPIB SRQ, or pulse out.

3.24 Options

Extended math and Measurement: Adds math and advanced measurements for all general purpose applications. Includes all standard math and measurement tools, plus the following tools:

3.25 Extended math tools

Automated measurements; Display any five parameters together with their average, high, low, and standard deviations.

absolute value	integrate
differentiate	square
exp (base e)	square root
exp (base 10)	trend (datalog)
log (base e)	histogram (200 events)
log (base 10)	

3.26 Cursor Measurements

Type	From	To
Relative time:	First point on waveform	Any other point on waveform
Relative voltage:	Select voltage level	Any other voltage level
Absolute time:	Time and voltage relative to	Ground and trigger
Absolute voltage	Voltage	Ground

3.27 Extended Measure Tools

cycle median
Δtime@level, % and volts
Δtime @level from trigger
Δtime from clock to data + (setup time)
Δtime from clock to data - (hold time)
fall @ level, % and volts
first point
last point
number of points
median
rise @ level, % and volts
std. Deviation
duration

3.28 WaveAnalyzer

Includes the Extended Math and Measure Tools as well as expanded capabilities for performing FFT's, averaging, histograms, and histogram paramters.

3.29 WaveAnalyzer Tools (Standard)

Histograms with 18 histogram parameters up to 2 billion events
Summed averaging to one million sweeps
FFT capability expands the basic FFT to include:
- FFT power averaging
- FFT power density – real and imaginary
- FFT on all acquisition points up to 25 Mpts

With Waveanalyzer FFT you get maximum resolution at wide frequency spans.

3.30 Other Application Solutions Available

Jitter and Timing Analysis (JTA)
Digital Filter Package (DFP)
PowerMeasure Analysis (PMA1)
Communications Mask Testing (MT01/MT02)
Polymask Mask Testing (PMSK)
Advanced Optical Recording Measurements (AORM) for LT37X scopes
Disk Drive Measurements (DDM)
PRML Analysis (PRML)

3.31 Free Software Utilities

ScopeExplorer: Easy-to-use utility that provides a simple but powerful way to control your scope remotely over RS-232-C, GPIB, or Ethernet.
ActiveDSO: Active X controls for flexible Windows applications programming with remote control.
MaskMaker: Create your tolerance mask offline with this graphic tool.
DSO Filter: Specify a set of filter coefficients offline and load them into the scope.

3.32 Basic Triggers

Edge/Slope/Window/Line: Triggers when signal meets slope and level condition

3.33 SMART Trigger Types

State/Edge qualified: Triggers on any input source only if a given state (or transition) has occurred on another source. Delay between sources is selectable by time or number of events.

Dropout: Triggers if the input signal drops out for longer than a selected time out between 25 ns and 20 s.

Pattern: Logic combination of 5 inputs (3 on 2 channel models); Each source can be high, low or don't care. Trigger entering or exiting the pattern.

TV: Triggers selectable fields (1,2,4 or 8) for NTSC, PAL SECAM, or non-standard video (up to 1500 lines).

3.34 SMART Triggers with Exclusion Technology

Signal or Pattern Width: Triggers on glitches or on pulse widths selectable from <2.5ns to 20 s or on intermittent faults.
Signal or Pattern Interval: Triggers on intervals selectable between 10 ns and 20 s
Slew Rate: Triggers on edge rates; select limits for dV, dt, and slope. Select edge limits between 2.5ns and 20s.
Runt: Positive or negative runts defined by two voltage limits and two time limits selectable between 2.5 ns and 20 ns

3.35 Hardcopy

Print Screen is activated by a front-panel button or via remote control. Store screen image files or print to external printers including network printers and directories. Netwrok printing and file access requires the LAN10BT Ethernet option.

Supported printers include:
B/W: LaserJet, DeskJet, Epson. An optional, internal high-resolution graphics printer is also availablefor screen dumps; stripchart output formats capable of up to 200 cm/div.
Color: DeskJet 550C, Epson Stylus, Canon 200/600/800 series, HP7470 and HP7550
Hard copy Formats: TIFF b/w, TIFF color, BMP color, BMP compressed and HPGL

3.36 Waveform Output

Store waveforms to floppy disk or optional PC-Card hard drives and memory cards.
Save any trace you choose and select Auto Store to automatically store the waveform after each trigger.
Output Formats: The ASCII waveform output is compatible with spreadsheets, MATLAB, MathCad, etc. Binary output is also available for reduced file size.

3.37 Documentation

Included with all WavePro Oscilloscopes: Operations Manual — hard copy, Remote Programming Manual — hard copy, CD-ROM — PDF formatted manuals plus software utilities including: ScopeExplorer, ActiveDSO, MaskMaker, DSO-Filter and DSO-Net Print Gateway.

4. Theory of Operation

4.1 Processor Board

MPC603e Processor

The PowerPC603e on the processor board is a 64-bit RISC processor having 2x32Kbyte cache and features high speed processing and quick memory access.
The processor is designed to operate with an internal clock which is 5 times the external bus clock cycles and is used under the 32bit mode.

The board consists of two circuit-blocks:

- The 32bit block, that contains the main PowerPC processor, synchronous dynamic RAM module, VGA interface, Super-I/O and main board interface.
- The 8bit block, which incorporates all peripherals and other interfaces for outer connections.

These two circuit-blocks are connected through MC68150 (dynamic bus sizer).

Power Supply

The board requires two power sources (Vcc and +12V). +12V source is used for OP-amps and small-peripheral operation.

The processor requires 3.3V and 2.5V, and some other logic devices are operated by the +5V source. All of the signals are TTL compatible.
An OP-amp and MOSFET transistor comprise the 3.3V and 2.5V power source. The reference voltage is taken through the voltage-resistor divider network across the +5V power source.

32bit Peripherals

There are 5 devices on the processor's 32bit data bus:

- VGA video controller
- S-DRAM system
- bus sizer, an interface to 8bit circuit-block
- Super-I/O
- MAIN board

CPU's Block Diagram

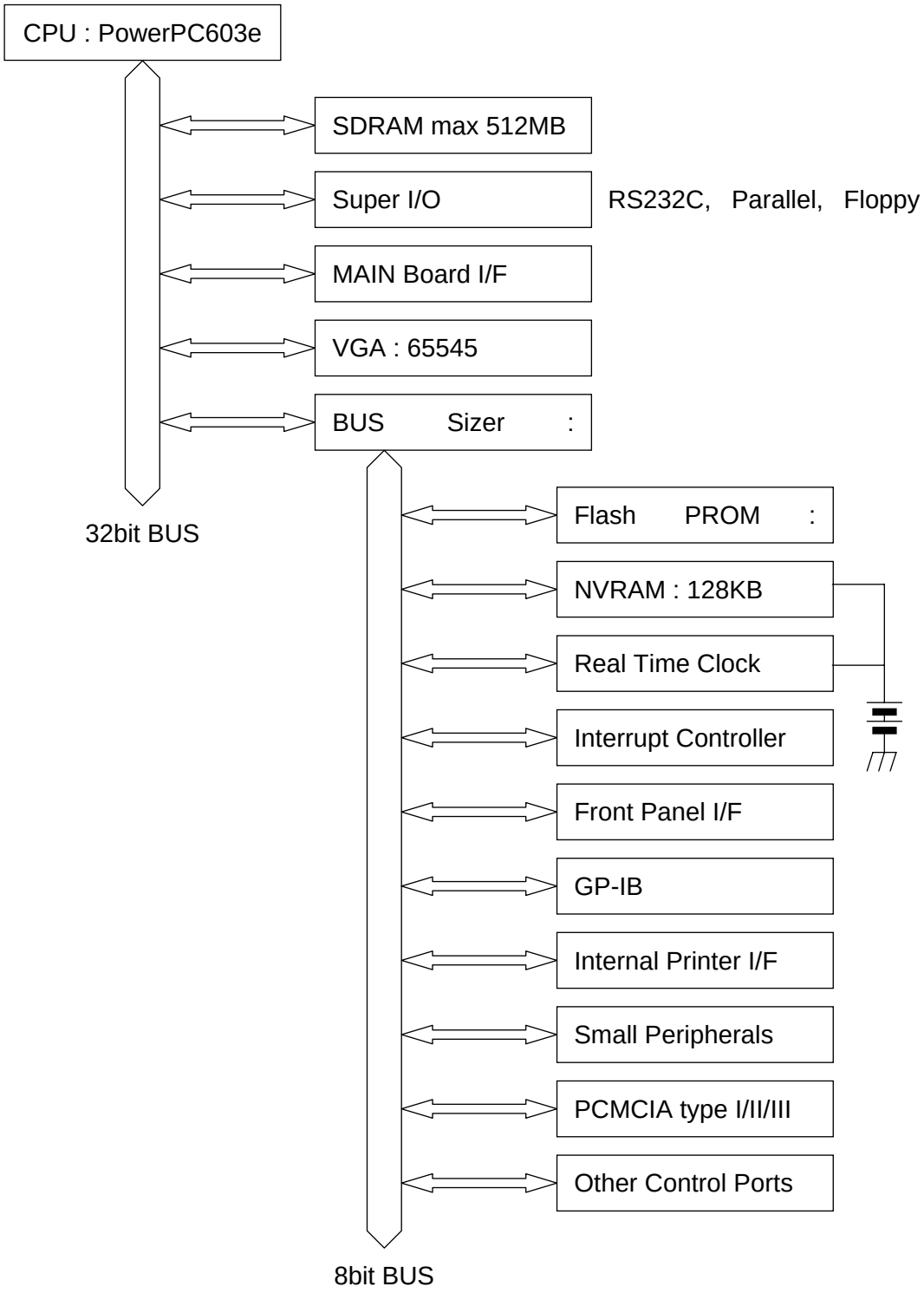


Figure 4-1 CPU Block Diagram

SDRAM

The SDRAM circuit consists of one DIMM module, from 64MB to a maximum of 512MB. The DIMM module type is 168pin SDRAM, 3.3V unbuffered CL=2. The SDRAM control circuit is built with one CPLD, and several gate ICs.

The SDM (IC87) located on the main control circuit generates all types of bus cycle timing (normal R/W, 2-beat/8-beat bursts of R/W), refresh cycles. Furthermore, the SDM has a register for setting the DIMM size, in order to adjust the memory mapping so as not to have gaps in memory mapping according with the memory capacity. Two multiplexers (IC9 and IC10) switch the address lines of odd and even addresses to be connected with the address lines of each DIMM.

Normal Access Timing

This is the simplest access possible: the processor puts an address onto the address bus and reads or writes the required data out of or to the SDRAM which corresponds with the bus. The bus width is 32bits, or 4bytes wide, and the CPU performs to read or write operations (of one through four bytes) which are chained in a bus cycle.

Burst Access Timing

A burst access, on the 603e configured with 32bit device operation, performs either two or eight successive reads in SDRAM (2-beat or 8-beat burst access). The idea is to put the beginning of an address onto the address bus and read/write data out of or to the SDRAM every clock cycle, without incrementing the address required by the processor (this is to be achieved by the SDRAM's Burst mode). The 8-beat access is indicated by an active "low" of NTBST signals and a 32bit access signal (SIZ2..0=011), and the 2-beat access is indicated by an active "high" of NTBST signals and an access size of 64 bits (SIZ2..0=100).

Refresh Timing

The 32 KHz clock from the RTC chip is used to generate the timing to refresh SDRAM. Without this clock, the SDRAM would not be refreshed and all the data in it would be erased. SDM detects the rising edge and the falling edge of this 32KHz clock. At the each edge, it generates the refresh cycles.

The arbitration logic between other accesses (bus cycle with the processor and DMA cycle) and refresh cycles reside in the SDM.

Memory Mapping

When power is turned on, the internal software automatically sets the system's memory size to the largest capacity available with the DIMM that is installed (64MB - 512MB DIMM size).

VGA controller

The VGA controller chip 65545(IC29) contains the logic circuits to decode its own addresses. It generates all the video signals (RGB, H/V, and all control lines to drive the flat panel), and controls its associated 1 MB video DRAM (to read, write and refresh). There are two 2Mb video DRAMs mounted but only 512KB of each of the DRAM's is used.

All timings are extracted from the 16MHz bus clock; therefore, no external crystal or time-base is required. The horizontal and vertical synchronization signals are sent to the external video connector (a half pitch, D-SUB15 pin connector is used).

The 65545 chip can support several bus interfaces (PCI, ISA, VL, etc), the system employs it for VL-bus applications with the mode of 256-color palette operations.

The controller has an 18bit color palette and can display 256 colors out of the available 260,000.

The power supply circuit for the liquid crystal panel has a MOSFET switch that switches the power supply of LCD to 3.3V or 5V.

Also the VGA controller has a switch, it switches the max signal level for the LCD to 3.3V or 5V.

Super-I/O

This device controls RS-232C, floppy disk, and parallel port operations. The controller has its own time-base with a 24MHz crystal. RS-232C can be used by simply connecting the MAX232 buffer (IC31) to it. Since the Super I/O chip has a 16-byte buffer, high speed data transfer is easily carried out.

A 2HD disk drive can be directly connected to the system without any external components other than a pull-up resistor; it can be operated in interruption mode.

The parallel interface is also activated without other external components other than a pull-up resistor, for the use of 2-way communication.

Bus Control

The BUS (IC93) performs all bus cycles except those for SDRAM. When the bus cycle starts, the MPC603e must terminate the bus cycle by returning signals after acknowledging each of the data and addresses, from the outside. The BUS is used to generate the acknowledgement signals.

Bus Sizer

The MPC603e processor does not support dynamic bus sizing, which is performed with the 68K processor family. Each 8bits of the 32bit bus is fixed or assigned with the lower addresses, or 0 through 3 bits. Therefore, if an 8bit device were directly connected to the bus, this device would be seen in 4byte steps each in the memory map area. To avoid this, the 8bit-bus peripheral unit is connected to the 32bit-bus through the bus sizer, MC68150 (IC15). The bus sizer divides one bus cycle for accessing 32 bit-bus of the processor into four cycles each of 8bit accessing cycle, and/or assigns 8bit-bus data to a corresponding 8bits within the 32bits.

8bit Peripherals

The following devices are listed as 8bit data bus units:

- PCMCIA Interface
- Flash PROM
- NVRAM
- RTC
- Interrupt Controller
- GPIB Interface
- Small-peripherals Interface
- Internal printer Interface
- Front-Panel I/F
- Other registers and ports

PCMCIA, type I/II/III interface

This interface consists mainly of buffers for both data and address busses. IC65 (D-F/F) holds control bits for the signals resetting the card, switching between the data area and the attribute area, and switching the card's modes. All bits in the register are reset to zero when the _RESET signal goes to active low, which means that their state is also guaranteed at power-up.

IC66 and the IC67 invert the most significant address bits of the memory card whenever the SWAP jumper is plugged in, so that the first bytes are always allocated to "FFF00000", regardless of the size of the memory card. This allows the processor to boot directly from the PCMCIA memory card used.

Flash PROM

Two pieces of Intel's 29F016-compatible 2MB PROMs (IC45 and 46) are used. These ICs do not require any programming voltage to write. From a hardware point of view, a flash PROM is regarded the same as an EPROM in read mode. To erase or write to memory, commands are written into the data bus. Writing and erasing must be performed by monitoring the status-signals (RY/#BY) on the port (IC49).

The program may be seen to start from the Flash PROM. The Flash PROM is, however, not regarded as the program or its program area even when start-up (even

when the screen appears) is completed, because the program must be processed in the SDRAM after transferring the program content from the Flash PROM into the SDRAM.

NVRAM

This memory chip is powered from V_{CCO} in the RTC. When the main power is off, the NVRAM is powered by the lithium battery, when it is on, it is powered from V_{CC}. The #CS1 signals are also controlled by the RTC. When the main power is turned off, the RTC sets the chip select "high" to place the SRAM in power-down mode to prevent any accidental overwriting. Stored panel setups (Setup1 - 4), the instruments last panel setup and trace memories M1-M4 are stored in the NVRAM.

RTC

The DS1689 real time clock has several functions:

- Keeps the time-of-day and current-date information while power is off.
- Generates the 32KHz clock for SDRAM refreshing.
- Generates a 128Hz periodic interrupt signal to force bus accessing from the processor and allow periodic updating of the time display.
- Provides a unique ID that identifies the origination of scope ID.
- Feeds the power and the chip select signal to the NVRAM.

The RTC chip generates timing clocks necessary for time keeping and other circuits using a 32.768KHz crystal. A few discrete components around the RTC leave it powered by the lithium battery when the system is turned off. When the system is turned on this circuit charges the battery. Accesses from the processor are done through bus separation circuit, since addresses and data are multiplexed. A unique ID is written into the RTC by the RTC manufacturer, since every chip must have a different value stored in it.

Interrupt Controller

In order to prioritize and control several interrupt sources, it is necessary to use an IC of uPD71059. It scans eight interrupt signals and sends a unique interrupt signal to the processor when an (unmasked) interrupt signal appears.
Interrupt levels are assigned as follows:

level 0	(lowest priority) FDC
level 1	small peripherals
level 2	RS232C
level 3	GP-IB
level 4	PCMCIA (I/O card mode)
level 5	real time clock
level 6	the MAIN board
level 7	(highest priority) unused

The priority in the above can be changed by the software.

Small Peripheral Interface

This 8-bit interface is intended to allow external expansion of the board in addition to the processor board. The tri-state buffers drive the address and control lines, and bi-directional buffers drive data lines. The address decoding is processed on each expanded peripheral board. Since the acknowledgement toward each access is also returned by the expanded board, there is no restriction to the amount of wait-states. The bus clock runs at 16MHz, and a reset line reinitializes the boards as does the CPU. Four interrupt lines are also included in this interface, so that interrupt-driven boards can be used.

Front Panel

The front panel is accessed by serial read/write signals passing through IC47 and IC48. The CPU board can be reset by resetting the 3 buttons on the front panel. This function becomes effective by setting a bit of IC52 for enabling. Both the LED and the beeper are activated by serial writing.

Reset Circuit

When the power supply is turned on and V_{CC} exceeds 4.5V, IC4 detects this and starts generating the clock (IC2) After the clock is stabilized and counted 1024 times, the reset signal is released by IC86 after the time determined by C167. Whenever V_{CC} goes below 4.5V (even for a very short time), a reset pulse, in which the width is determined by C6, is generated. Resetting 3 buttons on the front panel also cause the reset pulse as did IC4 when the supply power voltage fell too low.

Bus Error Generation

The MPC603e expects NTA and NAACK signals for acknowledgement to the current bus cycle, and inserts wait states during the period NTA and NAACK are kept at “high” levels (any of external devices have not pulled these signals "low"). As long as any of the devices do not return the acknowledgement, the bus is kept in this wait-condition. An external circuit is then required to generate a bus-error signal to break the pending cycle after a given time-out. The bus error is generated by pulling the NTEA pin of the CPU down to “low”. This job is done by the BUS (IC93) which counts the number of wait-states that have already passed through the counter. With this operation, the system can successfully force the termination of the current cycle. Some devices, such as the VGA video controller, have their own logic to generate a bus error. Therefore, any access operations for those devices do not need this circuit.

GPIB Interface

GP-IB controller is the National Instrument’s NAT4882. It has NEC-7210 software compatible made and it includes bus drivers.

Internal Printer Interface

Printer control is the same as for the normal Centronics interface. This circuit consists of buffers only.

Relation of I/O Structure to the associated CPLDs

The following block-diagram describes the flow in the decoder and the relationships between the acknowledgement to be returned to the CPU and CPLDs.

Three-line boxes are CPLDs, and one-line boxes indicate other ICs and function blocks.

- SDM does all the controls for the access of the SDRAM (Initialize memory, Decode and Mapping, Read/Write, Burst Read/Write, Refresh).
- Bus controls is the bus cycle of the entire CPU board. (Decode all areas other than SDRAM, Read/Write of 32bits bus, Read/Write of the bus via bus sizer, detection of bus error).

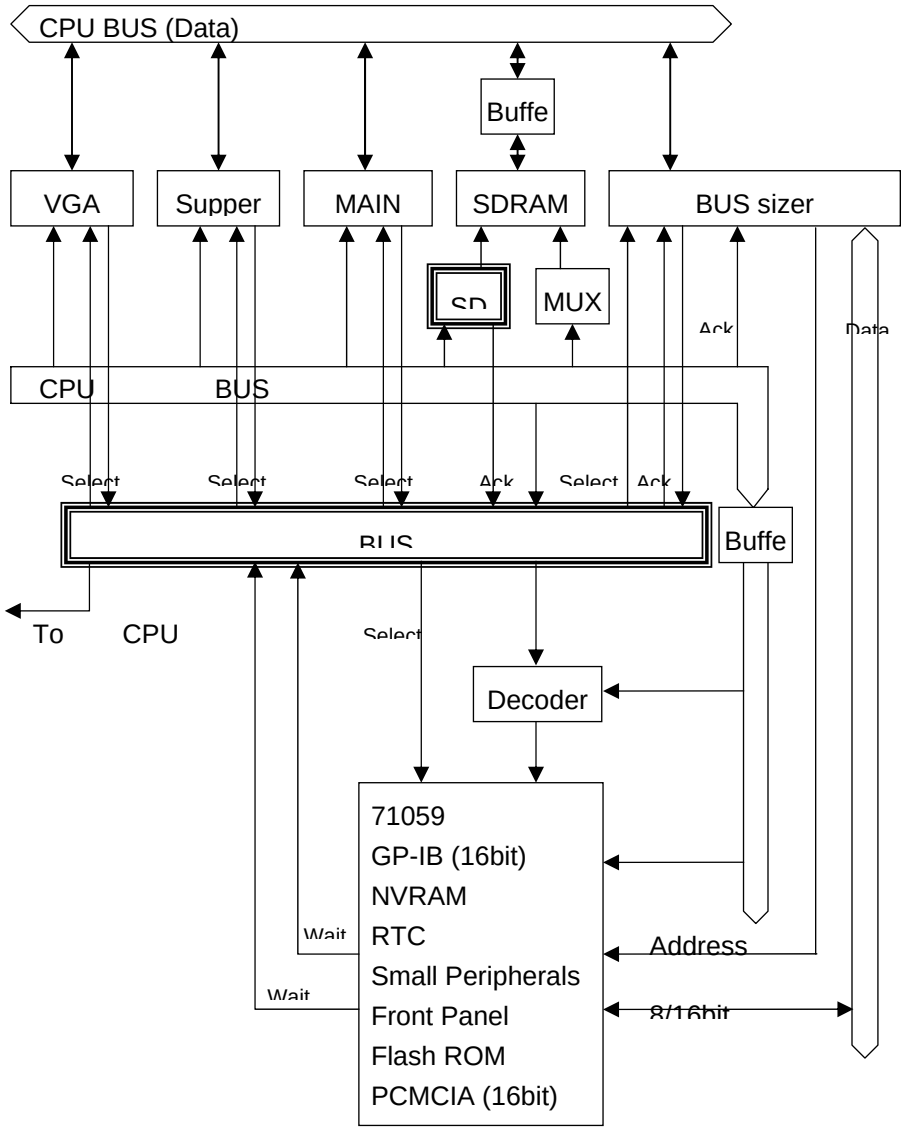


Figure 4-2 I/O Structure

4.2 Main Board

Introduction

The main board is divided into the following sections:

- **Front End**
  Based on the Hybrid HFE428, HSY632 switchyard to combine the input channels.
- **A/D Converter & Digital Acquisition Memory**
  Based on the HAM631.
- **Trigger**
  Based on the Hybrids HTR420 discriminator & MST429A smart trigger.
- **Timebase**
  Based on the MCG426 clock generator & MTB411A controller
- **Main Board Control**

4.2.1 Front End

The front end processes an analog signal for ADC and trigger, consists of High impedance buffer, amplifier HFE428, and trigger comparator HTR420.

The main functions of the Front end without the amplifier HFE428 and HTR420 are:

- Four channels opertion, calibration with Software control.
- Input protection (clamp+thermal detection) and coupling (AC, DC, 1MΩ, 50Ω).
- Attenuator by 10 & by 100.
- Offset control.
- Offset control of ±1V and CAL control of ±1.4V.
- Detection of 50Ω over loading.
- Input of signal for calibration.

The main functions of HFE428 are:

- Amplitude normalization for the ADC system : at the BNC the dynamic range is 16 mV to 80V FS (full scale) and the ADC/TRIG system input is 500 mV differential.
- Fine adjustment of gain and variable control
- Band width limiter of 20MHz, 200MHz

Main function of HFE420 are:

- Generation of trigger signal (analog input and digital output) with comparator
- Setting of trigger level (TRIG,VALIDATE)
- Setting of trigger coupling (DC,AC,LFREJ,HFREJ,HF)
- Setting of slope (+,-,WINDOW)

Control

Relay control

The relay of the attenuator is set by selecting the input coupling and the gain as shown in the table below.

RL1, 2 and 5 are driven with +5V/0V, and RL3, 4 is driven with +5V/-5V.

Input coupling

Control port	Relay	GND	1M,DC	1M,AC	50,DC
GND/*MES	RL2	H	L	L	L
1M/*50	RL1	H	H	H	L
AC/*DC	RL5	H	L	H	L
1/*10	RL3	H	X	X	X
1/*100	RL4	L	X	X	X

Switch of attenuator

Control port	Relay	2mV-99mV	100mV-0.99V	1V-10V
1/*10	RL3	H	L	L
1/*100	RL4	H	H	L

Divide gain

The gain ratio in each block and input range is a table below.

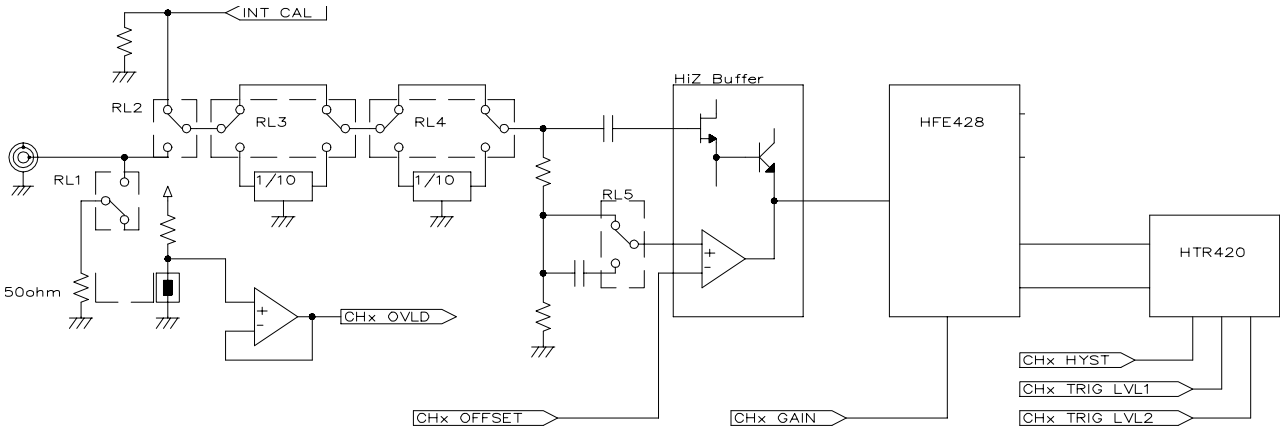
At the BNC the dynamic range is 16 mV to 80V FS (full scale) and the output is 500 mV differential (HAD631 input).

	Range V/div											
Block	2mV	5mV	10mV	20mV	50mV	100mV	200mV	500mV	1V	2V	5V	10V
ATT 1/*10	1	1	1	1	1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
ATT 1/*100	1	1	1	1	1	1	1	1	0.1	0.1	0.1	0.1
HFE428	31.25	12.5	6.25	3.125	1.25	6.25	3.125	1.25	6.25	3.125	1.25	0.625
Total(ratio)	31.25	12.5	6.25	3.125	1.25	0.625	0.3125	0.125	0.0625	0.03125	0.0125	0.00625

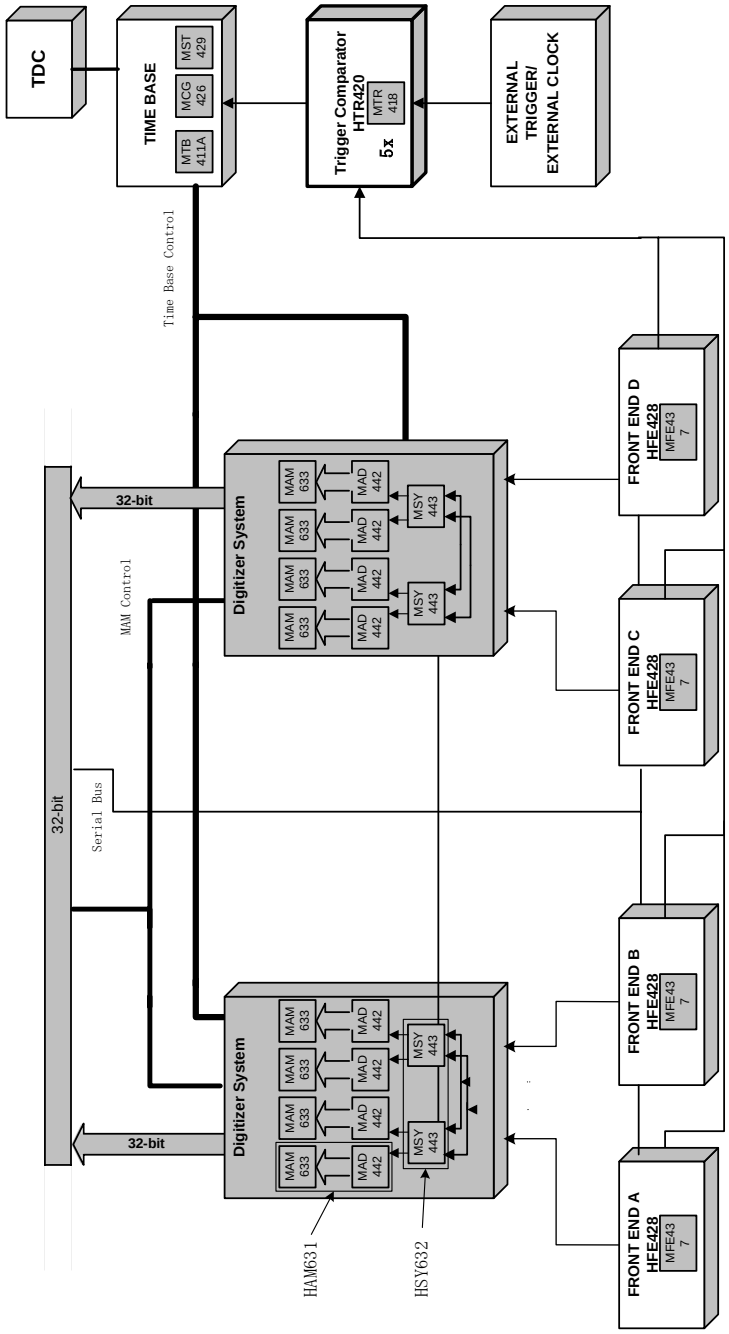
Analog control voltage

Circuit name	signal level	Signal name
CHx OFFSET	+/-4V	Offset control signal
CHx GAIN	0 to +4V	HFE428 gain control signal
CHx TRIG LVL1	+/-4V	Trigger level control signal
CHx TRIG LVL2	+/-4V	Trigger level control signal for smart trigger/window
CHx HYST	0 to +4V	Trigger hysteresis control signal
INT CAL	0 to +600mV	Signal each CH commonness for calibration

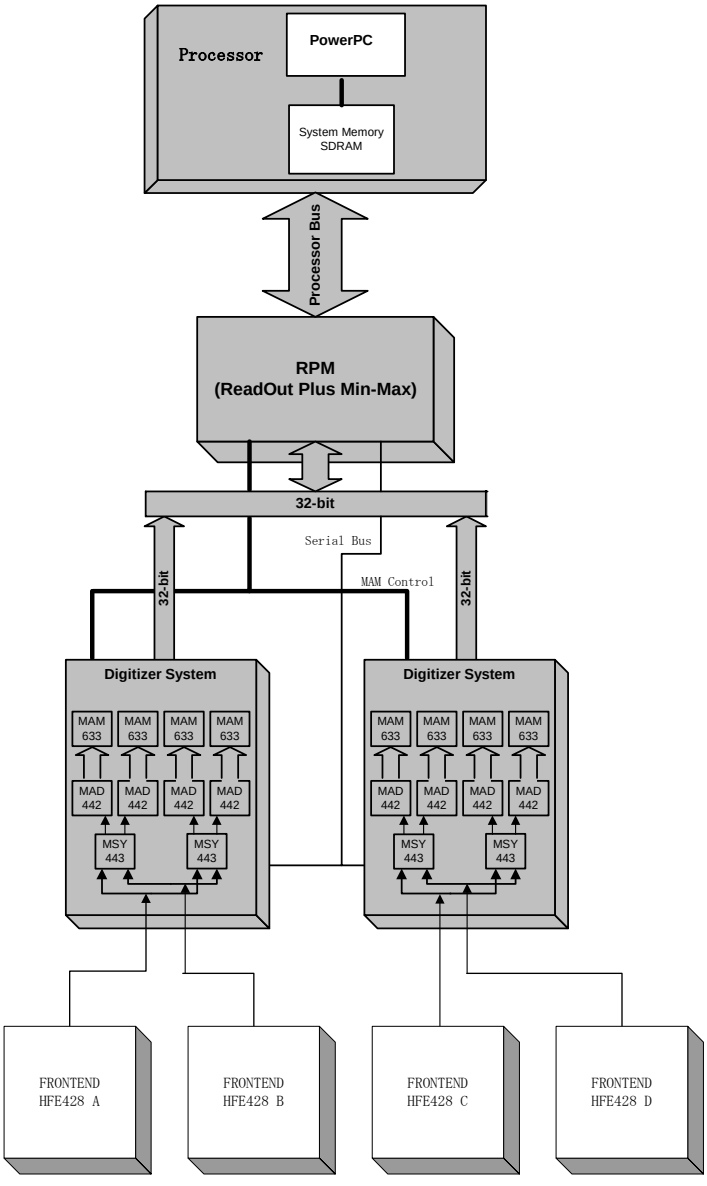
Block diagram 1



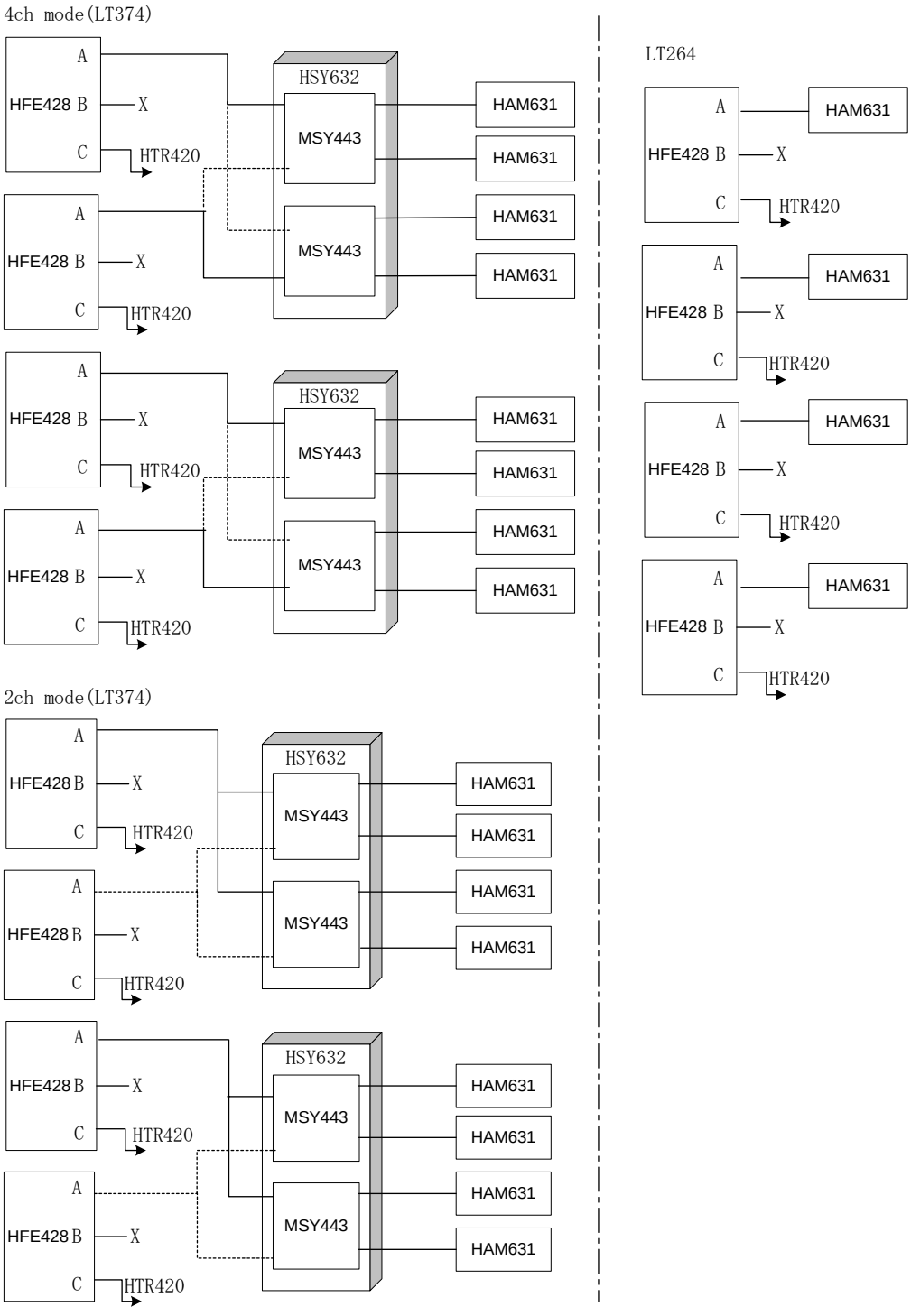
4.2.2 Acquisition Block Diagram



4.2.3 Control & Transfer Block Diagram



4.2.4 Channel Mode



4.2.5 µP Control

Control between the microprocessor and the main board is accomplished via the RPM. The RPM functions are:

- Processor interface
- MAM interface
- 8 bit bus interface (MTB411, MCG426, MST429A, IIC)
- Serial interface
- Min-Max Computation
- Histogram
- RPM is configured at boot up by the processor. The RPM configuration program is stored in the flash memory.

4.2.6 Trigger

The different trigger couplings are :

- DC
- AC : cut off frequency is almost 7.5 Hz.
- LF REJ : single pole high pass filter with a cut off frequency at 50 kHz.
- HF REJ : single pole low pass filter with a cut off frequency at 50 kHz.
- HF : frequency divider by four.

Analog Controls

A sample and hold fed by the precision DAC provides the threshold levels. A precision DAC is also used for a successive approximation ADC which measures Probus inputs, temperature, etc.

4.2.7 Analog to Digital Converter

Introduction

The analog to digital converter system does the signal conversion to 8 bits, using the following circuits:

- **HSY632:** Hybrid switching AMP 2 in 4 out.
- **HAM631**: Hybrid ADC 1GS/s with 4Mb memory. Provide 83 MHz clock for memory and refresh for DRAM

4.2.8 Time Base

Introduction

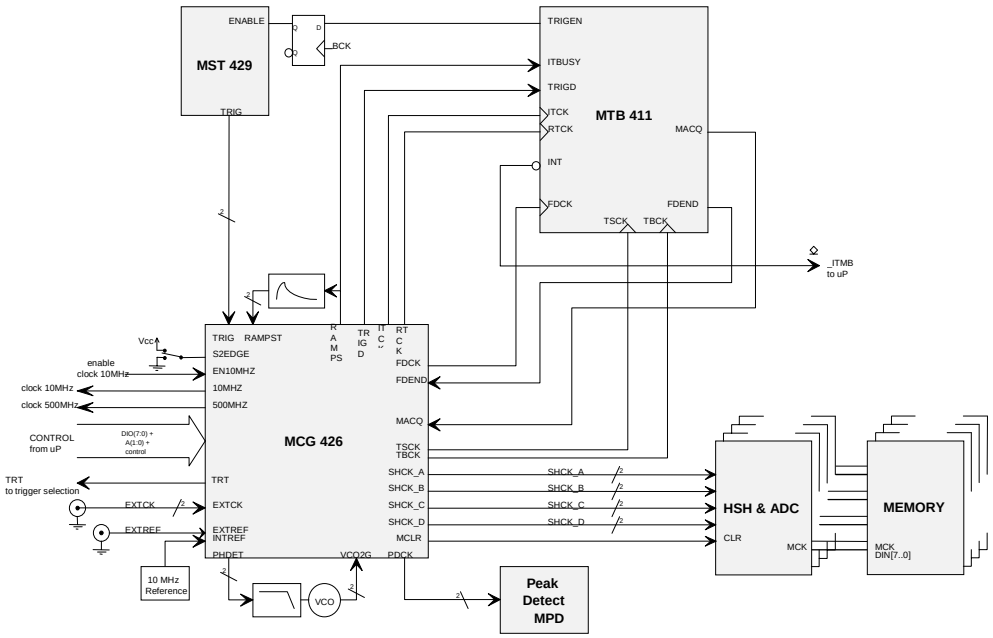
The time base includes three circuits:

- **MCG426**: generates sampling clocks: 12.5 MHz up to 2GHz
  generates clocks for the MTB411
  interleaves sampling clocks to increase sampling rate and memory depth.

- **MTB411A**: Time Base System
  TDC interpolator and Real Time computation
  Trigger circuitry
  Frequency divider

- **MST429A**: Single source trigger, Standard trigger, Hold off, Pulse width & interval
  Multiple source trigger, State qualified, Edge qualified

Block Diagram



Time Base Block Diagram

4.3 Power Supply

 Do not touch any electric parts inside the power supplies during operation as the primary side of the power unit has many high voltage portions to ground.

Input Voltages

The power supply supports a wide ranges of inputs, 90-132 V AC (45-440Hz) and 90-264V AC (45-66Hz) are allowed.

Output voltages: 9 different DC voltages are available, +5Vd, +12Vd, +12V, and +27V, +2.5Va, +5Va, -5Va, +12Va,–12Va.

Overview

The power supply unit consists of, roughly divided, Input Circuit, Input Filter & Rectification, Power Factor Correction, Main Converter (for digital circuits) , Main Converter (for analog circuits) and output regulators.

Power Switch

A power switch is located on the secondary side. In order to switch -on and -off all of the outputs on the secondary side; the control is made by switching on and off the main converter. When the power switch is off, some power is being fed to some components in the power supply unit (stand-by mode) as long as the unit is plugged into an AC source.

Cooling

The power supply is designed to use forced air cooling with a fan. Operating the power supply without a fan will cause the over-temperature protection circuits to trip because of the temperature rise in the unit. When the protection circuit trips the power outputs will be turned off.

5. Performance Verification

5.1 Introduction

This chapter contains procedures suitable for determining if the LT584, LT374/372, LT264/262 and LT354 Digital Storage Oscilloscope performs correctly and as warranted. They check all the characteristics listed in subsection 5.1.1.

Because they require time and suitable test equipment, you may not need to perform all of these procedures, depending on what you want to accomplish.

This manual performance verification procedure can be followed to establish a traceable calibration. It is the calibrating entities' responsibility to ensure that all laboratory standards used to perform this procedure are operating within their specifications and traceable to required standards if a traceable calibration certificate is to be issued for the Digital Storage Oscilloscope.

5.1.1 List of Tested Characteristics

This subsection lists the characteristics that are tested in terms of quantifiable performance limits.

- Input Impedance
- Leakage Current
- Noise
- DC Gain Accuracy
- Offset Accuracy
- Bandwidth
- Trigger Level
- Smart Trigger
- Time Base Accuracy

5.1.2 Calibration Cycle

The LT584, LT374/372, LT264/262 and LT354 Digital Storage Oscilloscope requires periodic verification of performance. Under normal use (2,000 hours of use per year) and environmental conditions, this instrument should be calibrated once a year.

5.2 Test Equipment Required

These procedures use external, traceable signal generators, DC precision power supply, step generator and digital multimeter, to directly check specifications.

Instrument	Specifications	Recommended
Signal Generator Radio Frequency	Frequency : .5 MHz to 2 GHz Frequency Accuracy : 1 PPM	HP8648B or equivalent
Signal Generator Audio Frequency	Frequency : 0 to 5 kHz Amplitude : 8 V peak to peak	LeCroy LW420 or HP33120A or equivalent
Voltage Generator DC Power Supply	Range of 0 to 20 V, in steps of no more than 15 mV	HP6633A or equivalent
Power Meter + Sensor	Accuracy ±1 %	HP437B + 8482A or equivalent
Digital Multimeter Volt & Ohm	Voltmeter Accuracy : 0.1 % Ohmmeter Accuracy : 0.1 %	Keithley 2000 or equivalent
Coaxial Cable, 1 ns	50Ω, BNC, length 20 cm,	LeCroy 480232001
Coaxial Cable, 5 ns	50Ω, BNC, length 100 cm,	LeCroy 480020101
2 Attenuators, 20 dB	50Ω, BNC, 1 % accuracy	LeCroy 402200402
Attenuator, 6 dB	50Ω, BNC, 1 % accuracy	LeCroy 402600403
Terminator, 2 W	50Ω, BNC, Feed-Through	LeCroy 402323001
T adapter	50Ω, BNC T adapter	LeCroy 402222002

Table 5-1 : Test Equipment

5.2.1 Test Records

The last pages of this document contain test records. Keep them as masters and use a photocopy for each calibration.

5.3 Turn On

If you are not familiar with operating the LT584, LT374/372, LT264/262 or LT354, refer to the operator's manual.

- Switch on the power using the power switch.
-
- Wait for a minimum of 20 minutes for the scope to reach a stable operating temperature, and verify:

The PNL files used depends on the scope model. The LTxxx represents the LT262, LT264, LT354, LT372, LT374. **For the LT584 use the LT374 files.**

5.4 Input Impedance

The impedance values for 50Ω and 1MΩ couplings are measured with a high precision digital multimeter. The DMM is connected to the DSO in 4-wire configuration (input and sense), allowing for accurate measurements.

Specifications & Test limits

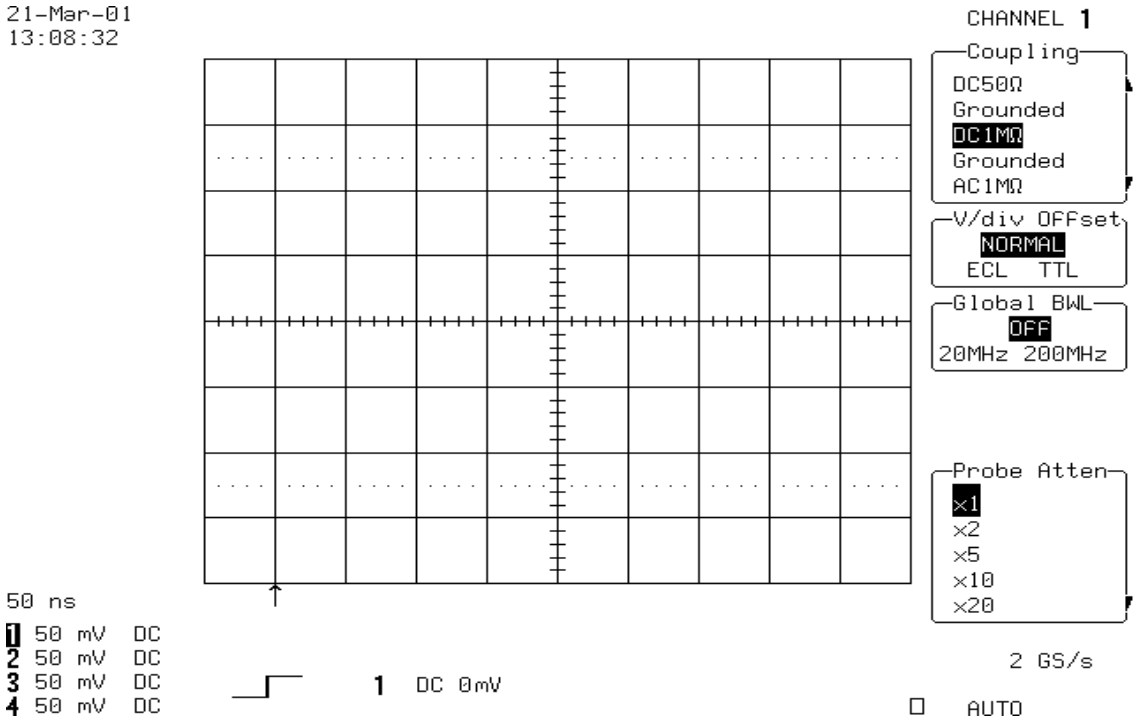
DC 1.00 MΩ ±1 %
AC 1.20 MΩ ±1 % (2mV/div to 99mV/div)
1.00 MΩ ±1 % (100mV/div to 10V/div)
DC 50Ω ±1 %

5.4.1 Channel Input Impedance

a. DC 1MΩ

- Recall **xxxP001.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	**50 mV/div.** on all 4 Channels
Time base	:	**50 nsec/div.**
Trigger mode	:	**Auto**

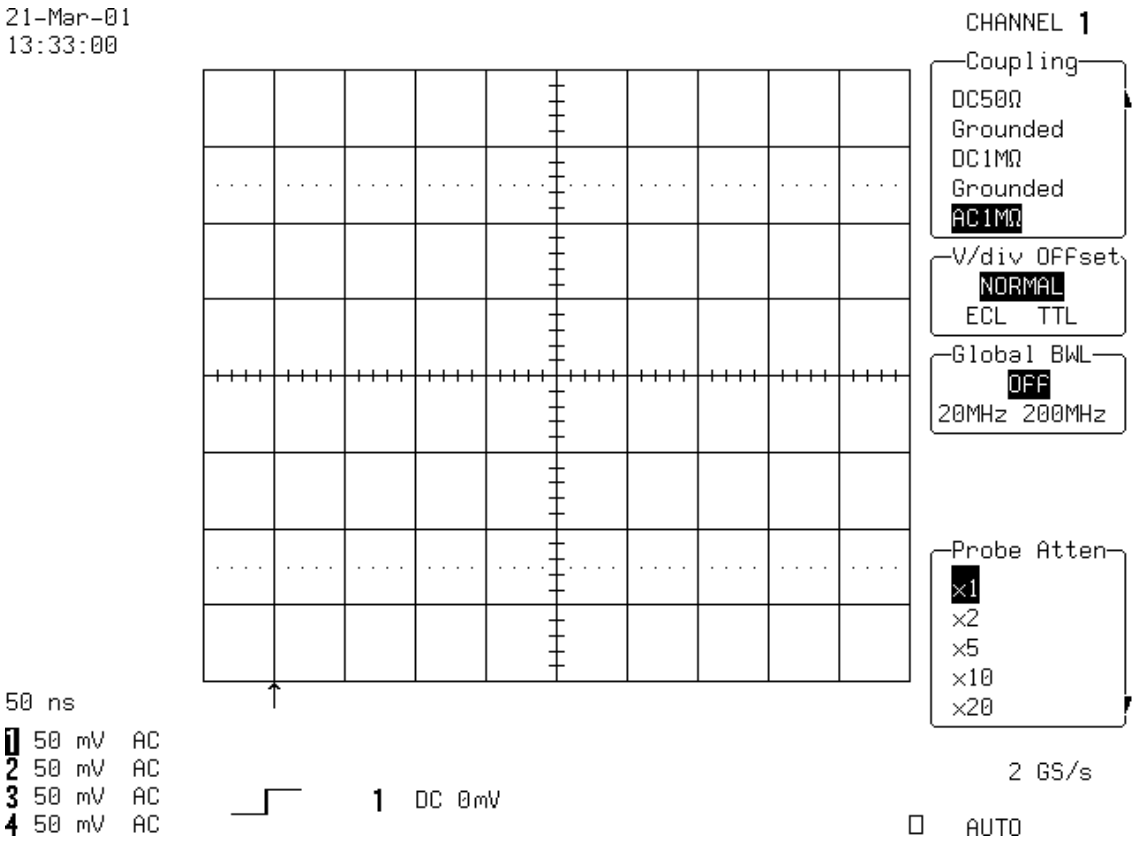


- Set the DMM with **Ohms and Ohms sense** to provide a 4 wire measurement.
- Connect it to Channel 1.
- Measure the **input impedance**. Record it in Table 2, and compare it to the limits.
- Repeat the above test for all input channels.
- Recall **xxxP002.PNL** or Set Input gain to **200 mV/div.** on all 4 Channels
- Repeat the test for all input channels.
- Record the measurements in Table 2, and compare the test results to the limits in the test record.

b. AC 1MΩ

- Recall **xxxP003.PNL** or configure the DSO as shown in 5.4.1.a, and for each Channel make the following change:

  Input Coupling : **AC 1MΩ**

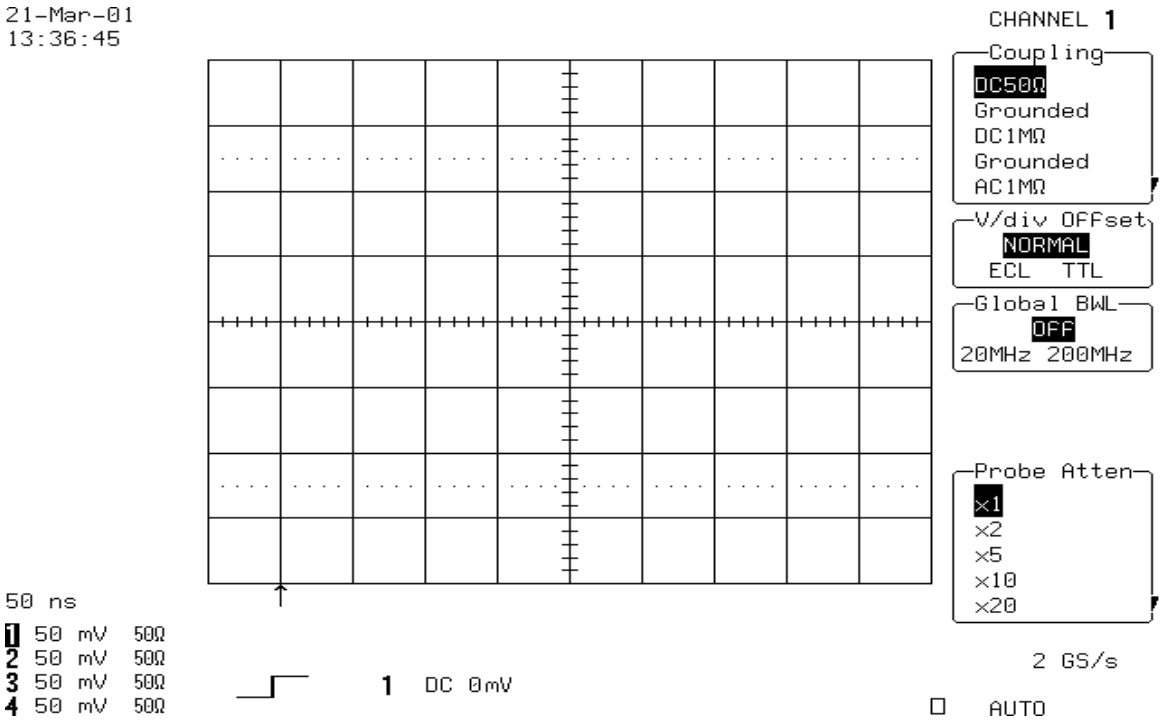


- For all input channels measure the **input impedance**.
- Record the input impedance in Table 2, and compare it to the limits.
- Recall **xxxP004.PNL** or Set Input gain to **200 mV/div** on all 4 Channels.
- Repeat the test for all input channels.
- Record the measurements in Table 2, and compare the results to the limits in the test record.

c. DC 50Ω

- Recall **xxxP005.PNL** or configure the DSO as shown in 5.4.1.a, and for each Channel make the following change:

  Input Coupling : **DC 50Ω**



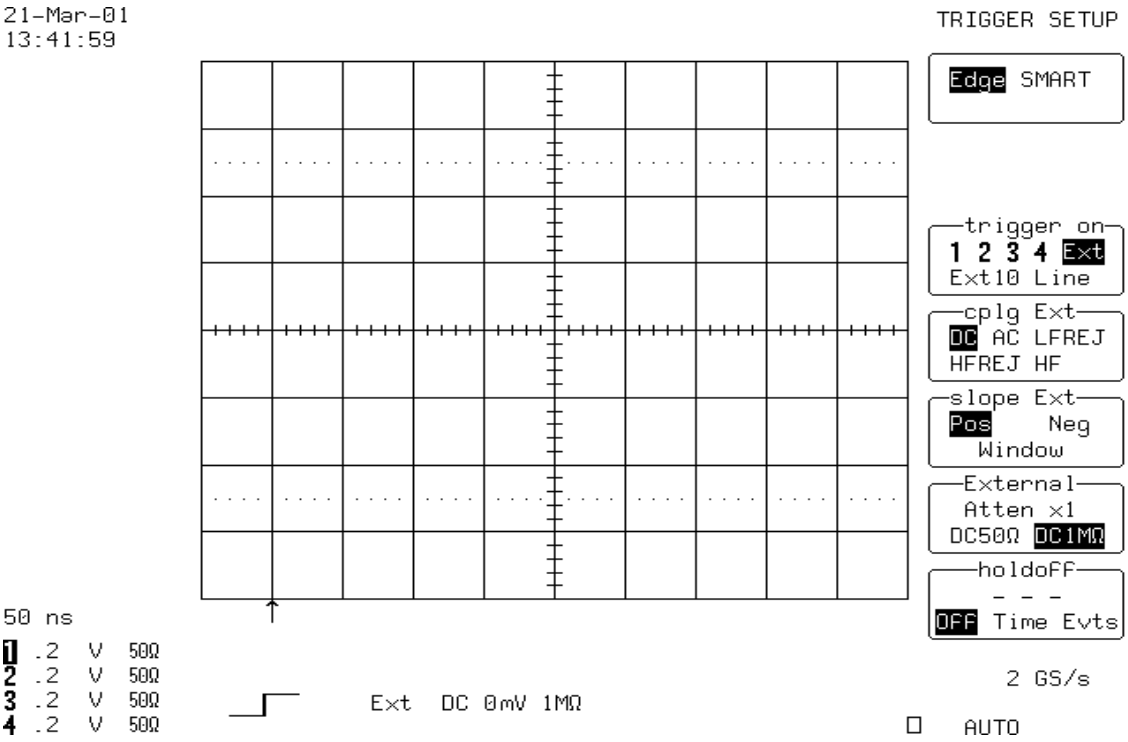
- For all input Channels, measure the input impedance.
- Record the **input impedance** in Table 2, and compare it to the limits.
- Recall **xxxP006.PNL** or set Input gain to **200 mV/div.** on all 4 Channels
- Repeat the test for all input channels. Record the measurements in Table 2, and compare the results to the limits in the test record.

5.4.2 External Trigger Input Impedance

a. DC 1MΩ

- Recall **xxxP007.PNL** or configure the DSO :

Trigger mode	:	**Auto**
Select Setup trigger		
Trigger on	:	**EXT**
Cplg Ext	:	**DC**
External	:	**DC 1MΩ**
Time base	:	**50 nsec/div.**



- Connect the DMM to External, and measure the **input impedance**.
- Record the input impedance in Table 2, and compare it to the limits.
- Recall **xxxP008.PNL** or set trigger to Ext/10
- Measure the **input impedance**.
- Record the test result in Table 2, and compare the result to the limits in the test record.

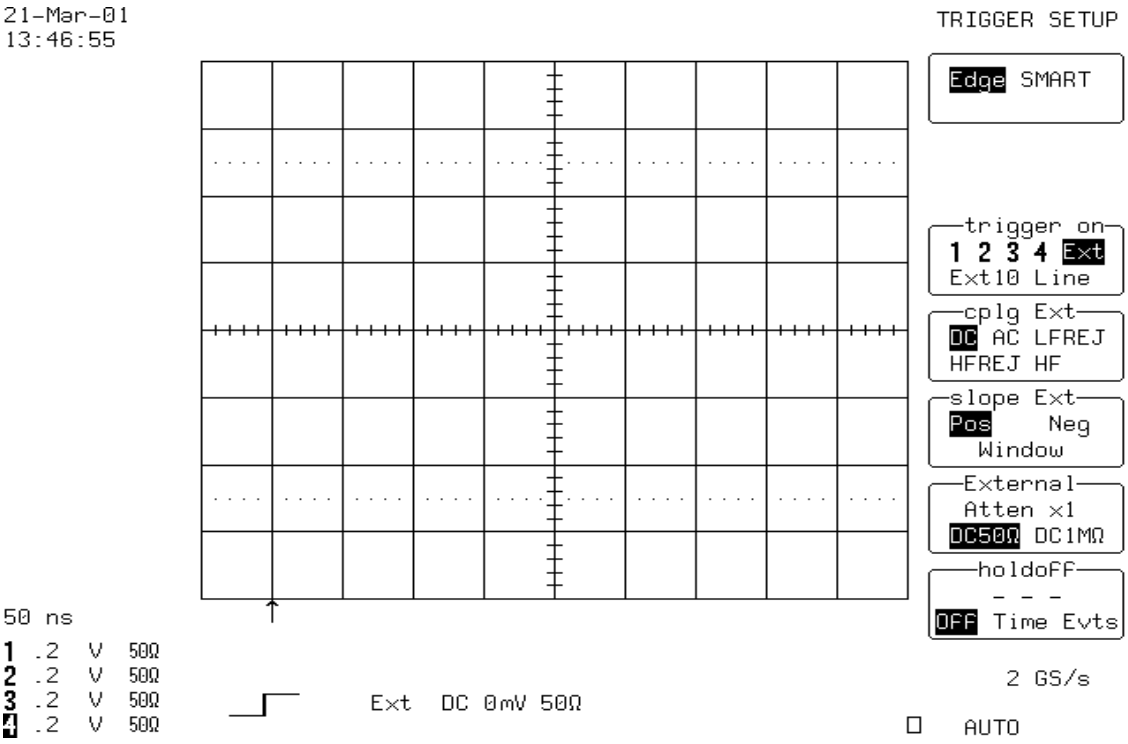
b. DC 50Ω

- Recall **xxxP009.PNL** or configure the DSO:

  Select Setup trigger

  Trigger on : **EXT**

  External : **DC 50Ω**



- Connect the DMM to External, and measure the **input impedance**.
- Record the input impedance in Table 2, and compare the result to the limit in the test record.

5.5 Leakage Current

The leakage current is tested by measuring the voltage across the input channel.

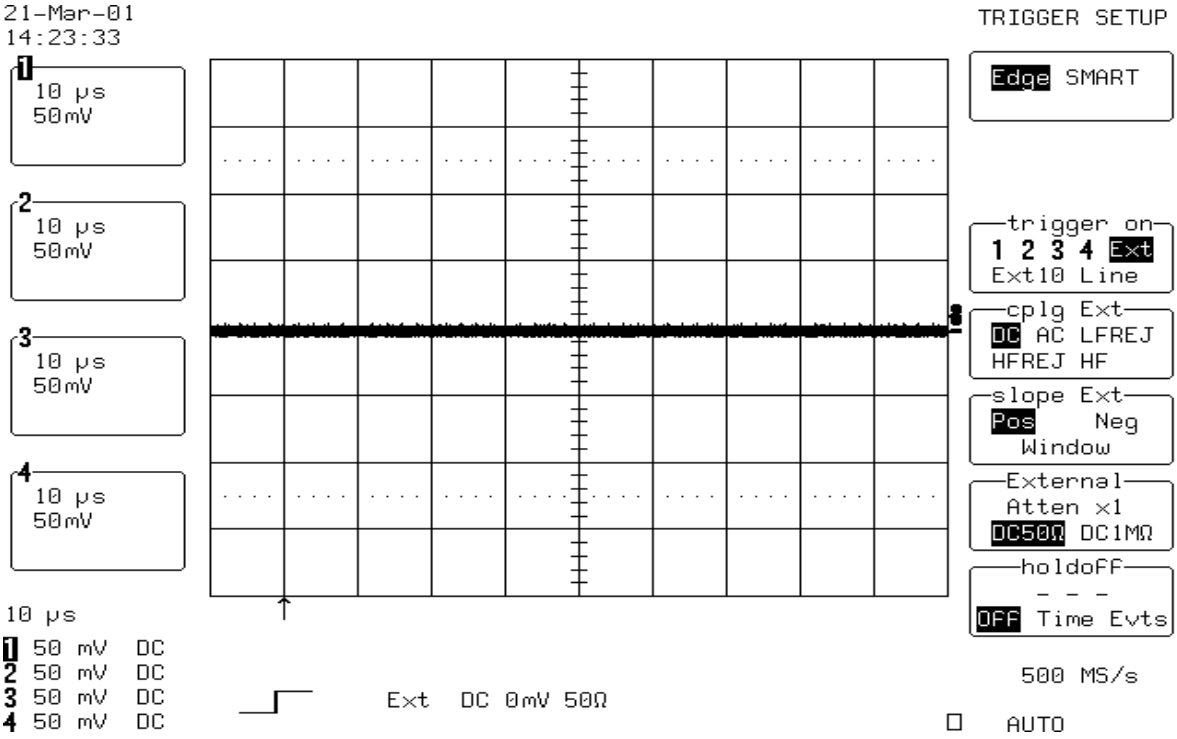
Test limit

DC 1MΩ : ±1 mV

5.5.1 Channel Leakage Current

- Recall **xxxP010.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	**50 mV/div.** on all 4 Channels
Trigger mode	:	**Auto**
Time base	:	**10 µsec/div.**



- Set the DMM to measure Volts, and connect it to Channel 1.
- Measure the **voltage** and enter it in Table 3. Compare it to the limits.
- Repeat the test for all input channels.

5.5.2 External Trigger Leakage Current

a. DC 50Ω

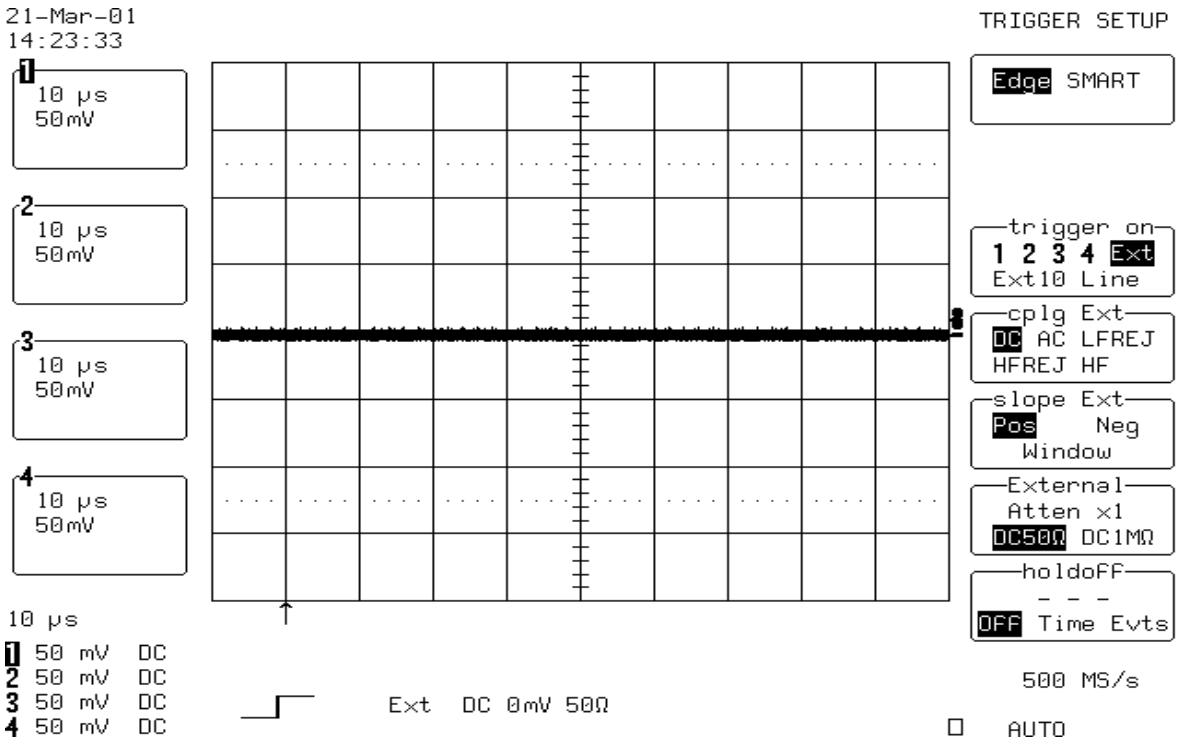
- Recall **xxxP011.PNL** or configure the DSO as shown in 5.5.1 and make the following changes :

  Select Setup trigger
  Set Trigger on : **EXT**

  External : **DC 50Ω**

- Connect the DMM to External.

- Measure the **voltage** and enter it in Table 3. Compare it to the limits.



5.6 Noise

Noise tests with open inputs are executed on all channels for both 1MΩ and 50Ω input impedance, with AC and DC input coupling, 0 mV offset, at a gain setting of 5mV/div., and different Time base settings.
The scope parameters functions are used to measure the RMS amplitude.

5.6.1 Rms Noise

Test limits

0.5 mV rms at 10 mV/div	LT37x
0.45 mV rms at 10 mV/div	LT354, 26x.

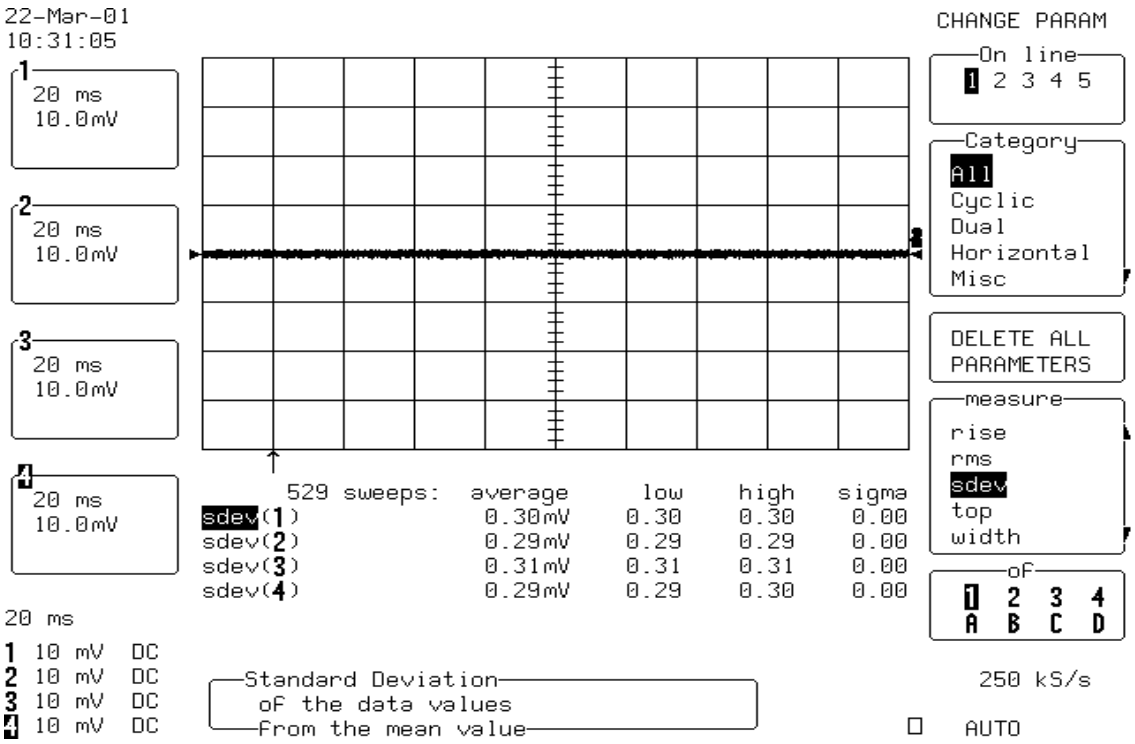
Procedure

a. DC 1MΩ

With no signal connected to the inputs

- Recall **xxxP012.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	**10 mV/div.** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**1**
Coupling 1	:	**DC**
Trigger Mode	:	**Auto**
Time base	:	**20 msec/div.**
Channel use	:	**4**
Record up to	:	**50 k Samples**
Press	:	**WAVE PILOT**
Measure	:	**MEASURE**
Mode	:	**Custom**
Statistics	:	**On**
Change parameters		
Category	:	**All**
On line 1	:	**Measure sdev of Ch1**
On line 2	:	**Measure sdev of Ch2**
On line 3	:	**Measure sdev of Ch3**
On line 4	:	**Measure sdev of Ch4**
On line 5	:	**no parameter selected for line 5**



- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.
- Record the four **high sdev** parameter values in Table 4, and compare the test results to the limits in the test record.
- Repeat the test for Time base : **1 msec/div.**, **50 µsec/div.**, and **2 µsec/div.**
- Record the measurements (high sdev of 1,2,3,4) in Table 4, and compare the results to the limits in the test record.

b. AC 1MΩ

- Recall **xxxP013.PNL** or configure the DSO as shown in 5.6.1

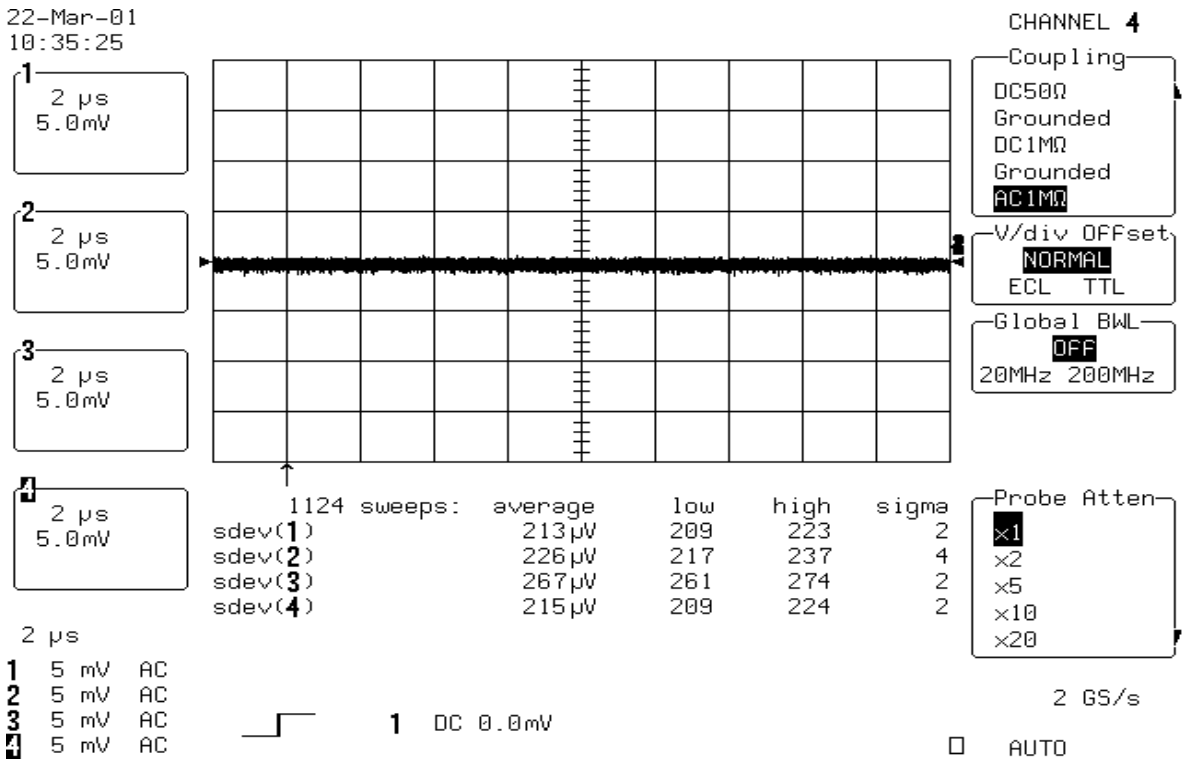
and for each Channel make the following change :

Input Coupling : **AC 1MΩ** on all 4 Channels
Input gain : **5 mV/div.** on all 4 Channels

Time base : **2 µsec/div.**

- Press **Clear Sweeps.**
- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.

- Record the four **high sdev** parameter values in Table 4, and compare the test results to the limits in the test record.



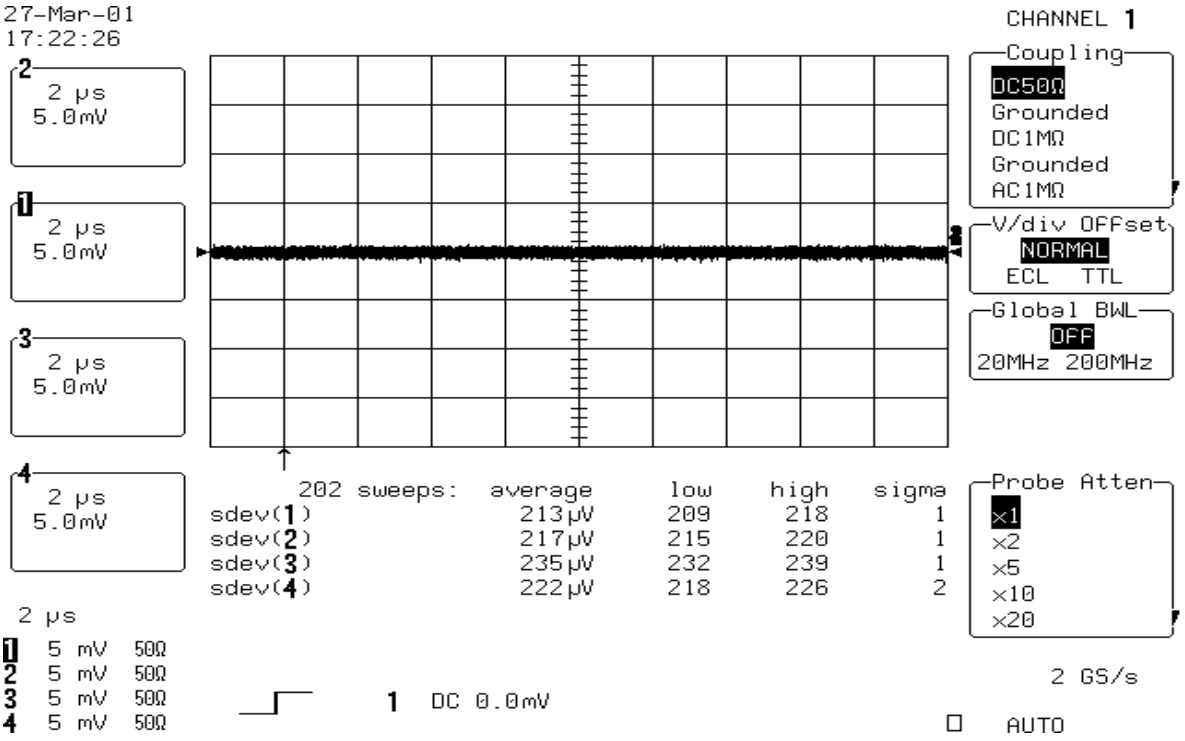
c. DC 50Ω

- Recall **xxxP014.PNL** or configure the DSO as shown in 5.6.1 and make the following changes :

  Input Coupling : **DC 50Ω** on all 4 Channels
  Input gain : **5 mV/div.** on all 4 Channels

  Time base : **2 µsec/div.**

- Press **Clear Sweeps.**



- Measure for at least **50 sweeps**, then press **Stop** to halt the acquisition.

- Record the four **high sdev** parameter values in Table 4, and compare the test results to the limits in the test record.

- Repeat the test for Time base : **20 µsec/div.**

- Record the measurements (high sdev of 1,2,3,4) in Table 4, and compare the results to the limits in the test record.

5.7 DC Accuracy

This test measures the DC Accuracy of the absolute voltage measurements at 0V offset setting. It requires a DC source with a voltage range of 0 V to 20 V adjustable in steps of no more than 15 mV, and a calibrated DMM that can measure voltage to 0.1 %. Measurements are made using voltage values applied by the external voltage reference source, measured by the DMM, and in the oscilloscope using the parameters Std voltage.
For each known input voltage, the deviation is checked against the tolerance.

Specification & Test limits

±(0.015 x | Vm + Voffset | + 0.015 x | Voffset| + 0.01 x FS + 1mV)

Vm [volts] = voltage reading [volts]
FS [volts] = 8[div] x sensitivity [volt/div]
Voffset [volts] = setting offset voltage [volts]

Procedure

- Recall **xxxP018.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input offset	:	**0.0 mV** on all 4 Channels
Input gain	:	from **2mV/div to 1 V/div and 5V/div.** (see Table 6) on all 4 Ch
Trigger setup	:	**Edge**
Trigger on	:	**line**
Slope line	:	**Positive**
Mode	:	**Auto**
Time base	:	**2 msec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
ANALYSIS CONTROL		
Trace ON	:	**A, B, C & D**
MATH TOOLS		
For Math	:	**Use at most 5000 points**
Redefine A, B, C, D		**Channel 1, Channel 2, Channel 3 & Channel 4**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**100 sweeps**
WAVE PILOT	:	**MEASURE**
Mode	:	**Custom**
Statistics	:	**off**
Change parameters		
On line 1	:	**Measure mean of A**

On line 2 : **Measure mean of B**
On line 3 : **Measure mean of C**
On line 4 : **Measure mean of D**

- For the low sensitivities: **2 mV, 5 mV, 10 mV and 20 mV/div**., connect the test equipment as shown in Figure 5-1.

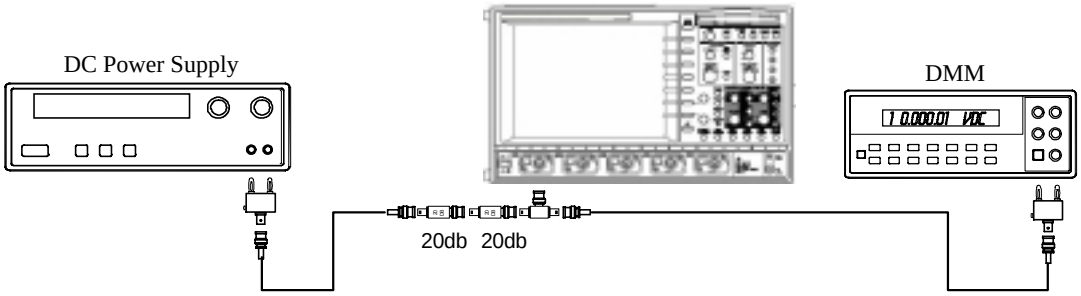


Figure 5-1: DC 1MΩ Accuracy Equipment Setup for 2,5,10 and 20 mV/div.

- For 50 mv/div & 100 mV/div, connect the test equipment as shown in Figure 5-2.
- For 5V/div, no attenuator is required, connect the test equipment as shown in Figure 5-3.

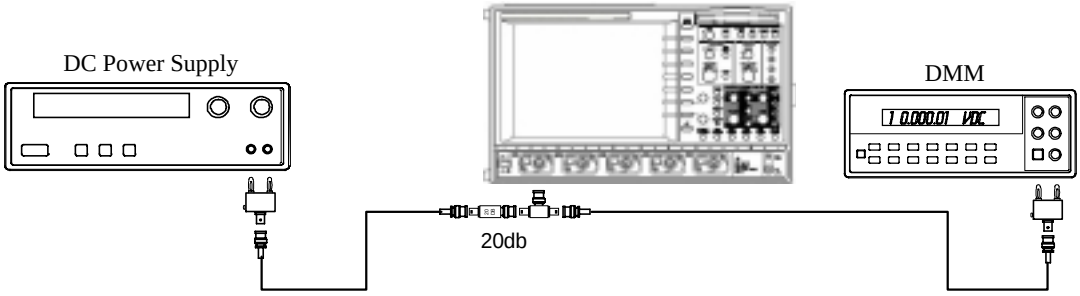


Figure 5-2: DC 1MΩ Accuracy Equipment Setup for 100 mV/div

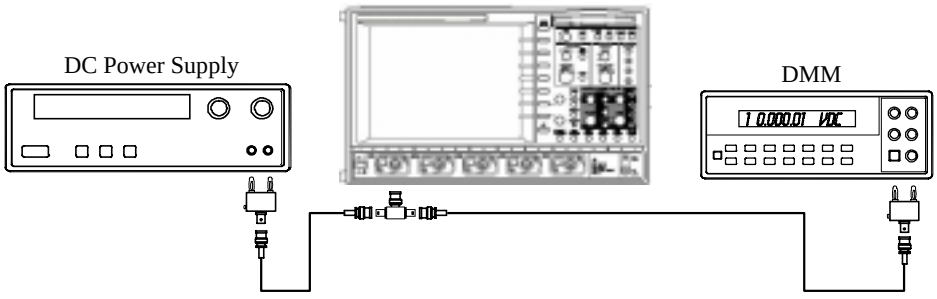


Figure 5-3 : DC 1MΩ Accuracy Equipment Setup for 5V/div.

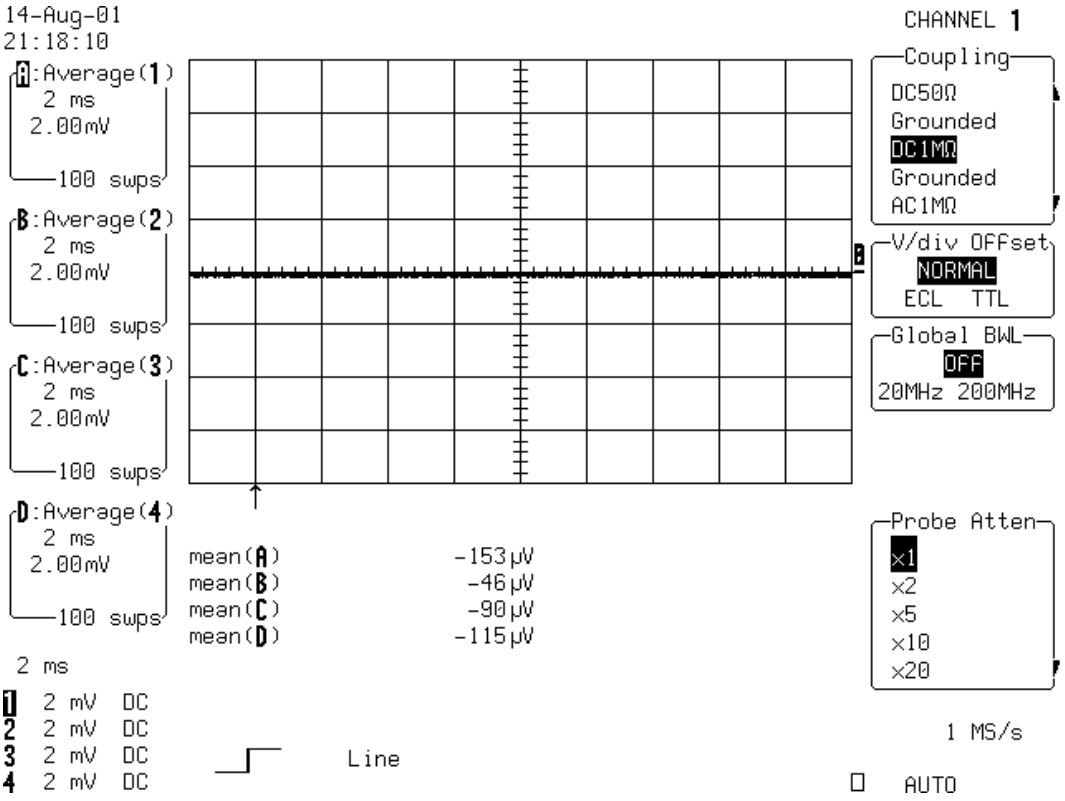
- For each **DSO Volts/div**, set the output of the external **DC voltage reference source** as shown in Table 5, column PS output.

1) Connect the DMM and record the **voltage reading** in Table 6, column **DMM.**

2) Press **Clear Sweeps**

3) After 10 sweeps, read off the **DSO mean parameter**, and record the measurement in Table 5, column **Mean**.

- For each DC voltage applied to the DSO input, repeat parts 1), 2), 3) and 4).
- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading. Record the test result in Table 5, and compare the **Difference (Δ)** to the corresponding limit in the test record.
- Repeat step 5.7 Procedure for the other channels, substituting channel controls and input connector.



5.8 Offset Accuracy

The offset test is done at 5mV/div, with a signal of ±1 Volt cancelled by an offset of the other polarity.

Specifications

± (0.015 x Voffset + 0.005 x FS + 1mV)

FS [volts] = 8[div] x sensitivity[volts/div]
Voffset [volts] = setting offset voltage

Procedure

- Recall **xxxP019.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 1MΩ** on all 4 Channels
Input gain	:	5**mV/div** on all 4 Channels
Input offset	:	**+1 Volt** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**1**
Coupling 1	:	**DC**
Mode	:	**Auto**
Time base	:	**2 msec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
ANALYSIS CONTROL		
Trace ON	:	**A, B, C & D**
Select MATH TOOLS		
For Math	:	**Use at most 5000 points**
Redefine A, B, C, D		**Channel 1, Channel 2, Channel 3 & Channel 4**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**100 sweeps**
WAVE PILOT	:	**MEASURE**
Mode	:	**Custom**
Statistics	:	**off**

- Connect the test equipment as shown in Figure 5-4.

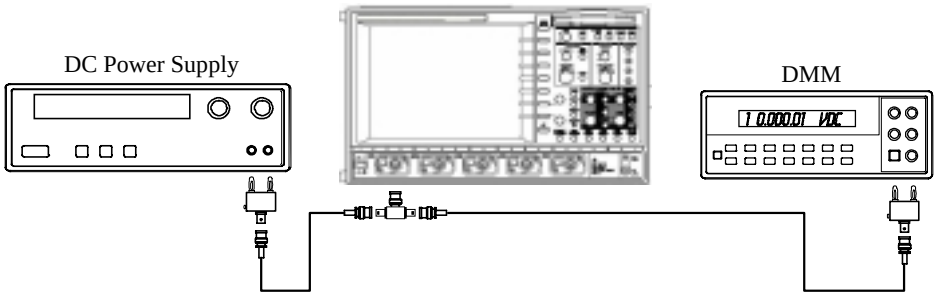


Figure 5-4 Offset Accuracy Test Setup

- Set the output of the external **DC voltage reference source** to **–1 Volt**. (or reverse the polarity of the banana jack adapter if the supply does not have bipolar outputs)

  1) Verify that the displayed trace A : Average (1) is on the screen, near the center horizontal graticule line. If the trace is not visible, modify the **DC voltage reference source output** until the trace is within ± 2 divisions of center.

  2) Connect the DMM and record the **voltage reading** in Table 6, column **DMM**.

  3) Disconnect the DMM from the BNC T connector.

  4) Press **Clear Sweeps**

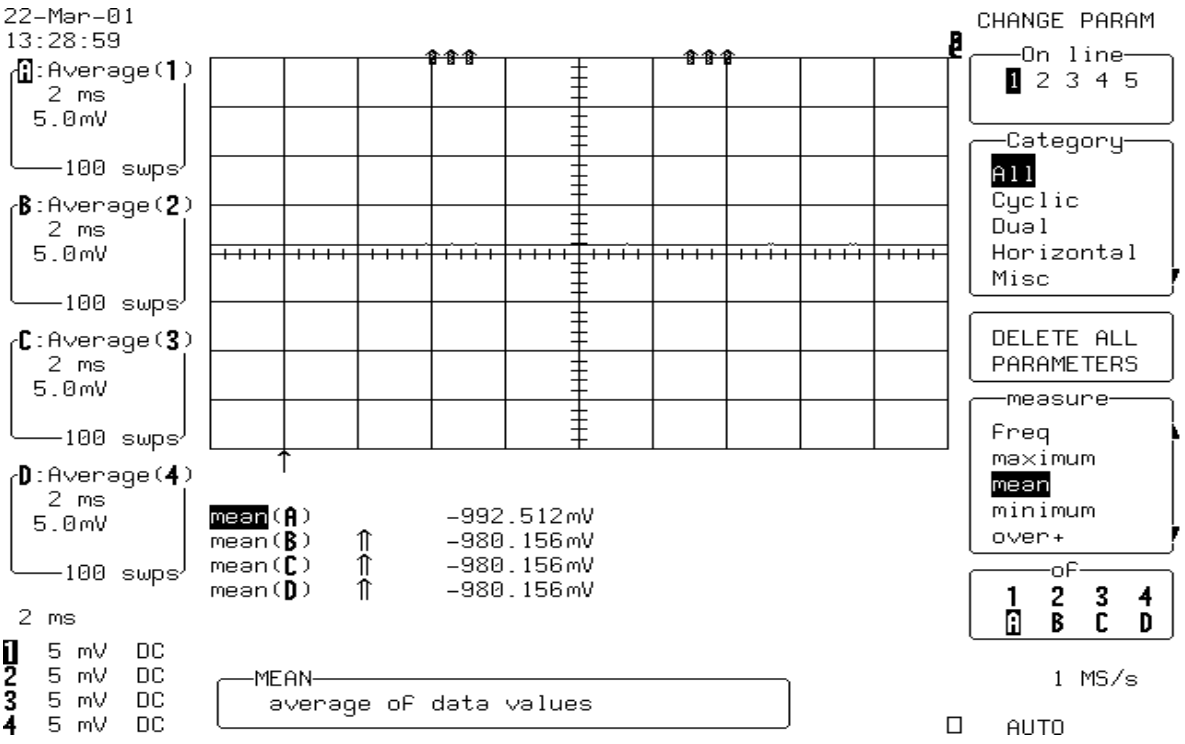
  5) After 10 sweeps, Read off the **DSO Mean parameter** voltage, and record the measurement in Table 6, column **Mean**.

- Repeat the test for the other channels, substituting channel controls and input connector. Record the measurements in Table 6.

- Repeat the test the other offset settings –1V and 0V.
  Recall **xxxP020.PNL** for Input offset –1V.
  Recall **xxxP021.PNL** for Input offset 0V.
  Record the measurements in Table 6.

- Calculate the **Difference (Δ)** by subtracting the **DMM voltage** reading from the **DSO mean** voltage reading.

- Record the test result in Table 6, and compare the **Difference (Δ)** to the corresponding limit in the test record.


22-Mar-01
13:28:59
A:Average(1)
2 ms
5.0mV
100 swps
B:Average(2)
2 ms
5.0mV
100 swps
C:Average(3)
2 ms
5.0mV
100 swps
D:Average(4)
2 ms
5.0mV
100 swps
2 ms
1 5 mV DC
2 5 mV DC
3 5 mV DC
4 5 mV DC
mean(A) -992.512mV
mean(B) -980.156mV
mean(C) -980.156mV
mean(D) -980.156mV
MEAN
average of data values
CHANGE PARAM
On line
1 2 3 4 5
Category
All
Cyclic
Dual
Horizontal
Misc
DELETE ALL PARAMETERS
measure
Freq
maximum
mean
minimum
over+
of
1 2 3 4
A B C D
1 MS/s
AUTO

5.9 Bandwidth

The purpose of this test is to ensure that the entire system meets the bandwidth specification. An external source is used as the reference to provide a signal where amplitude and frequency are well controlled.
If a leveled sine wave generator is not used then the amplitude of the generator as a function of frequency and power must be calibrated using an HP8482A sensor on an HP437B power meter or equivalent.

Specifications & Test limits

DC to 1GHz (10mV to 5V/div)	LT584
DC to 500MHz (10mV to 5V/div)	LT37x, LT354
DC to 350MHz (10mV to 5V/div)	LT26x

Procedure

- Recall **xxxP022.PNL** or configure the DSO

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 50Ω** on all 4 Channels
Input gain	:	**50 mV/div** on all 4 Channels
Input offset	:	**0 mV** on all 4 Channels
Trigger setup	:	**Edge**
Trigger on	:	**Line**
Slope line	:	**Positive**
Mode	:	**Auto**
Time base	:	**1 µsec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
WAVE PILOT	:	**MEASURE**
Mode	:	**Custom**
Statistics	:	**On**
Change parameters		
On line 1	:	**Sdev of 1**
On line 2	:	**Sdev of 2**
On line 3	:	**Sdev of 3**
On line 4	:	**Sdev of 4**

- Connect the HP8482A power sensor to the power meter.
- Zero and **calibrate** the power sensor according to the power meter instructions.
- Connect a **BNC adapter** to the power sensor.

- Connect a 5ns 50Ω BNC cable to the **RF output** of the HP8648B generator and then through a 6dB attenuator and the necessary adapters to the power sensor.

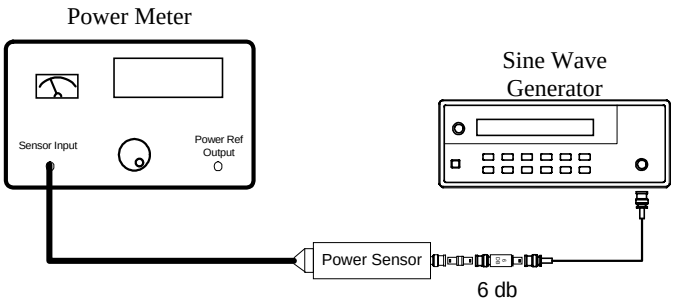


Figure 5-5 : Power Meter Equipment Setup

- Set the generator frequency to **300 kHz**

- Set the power meter to the correct **Correction Factor**

- Set the generator amplitude to measure **0.200 mW** on the power meter.

- Read the displayed **generator output amplitude**, and record it in the third column of Table 7.

- Repeat the above measurement for 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz & 500.1 MHz (changing the correction factor of the power meter at each frequency). Record the generator output amplitude readout in the third column of Table 7 for LT37X or LT354. For LT26X, use Table 7A for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 175.1 MHz & 350.1 MHz. For LT584, use Table 7B for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz, 500.1 MHz & 1000.1 MHz.

- Disconnect the **RF output** of the HP8648B generator from the HP8482A power sensor.

- Connect the **RF output** of the HP8648B generator through a 5ns 50 Ohm BNC cable and a 6 dB attenuator into Channel 1.

- Set the generator frequency to **300 kHz**.

- From the generator, apply the **recorded generator signal amplitude** to Channel 1.

- Press **Clear Sweeps**.

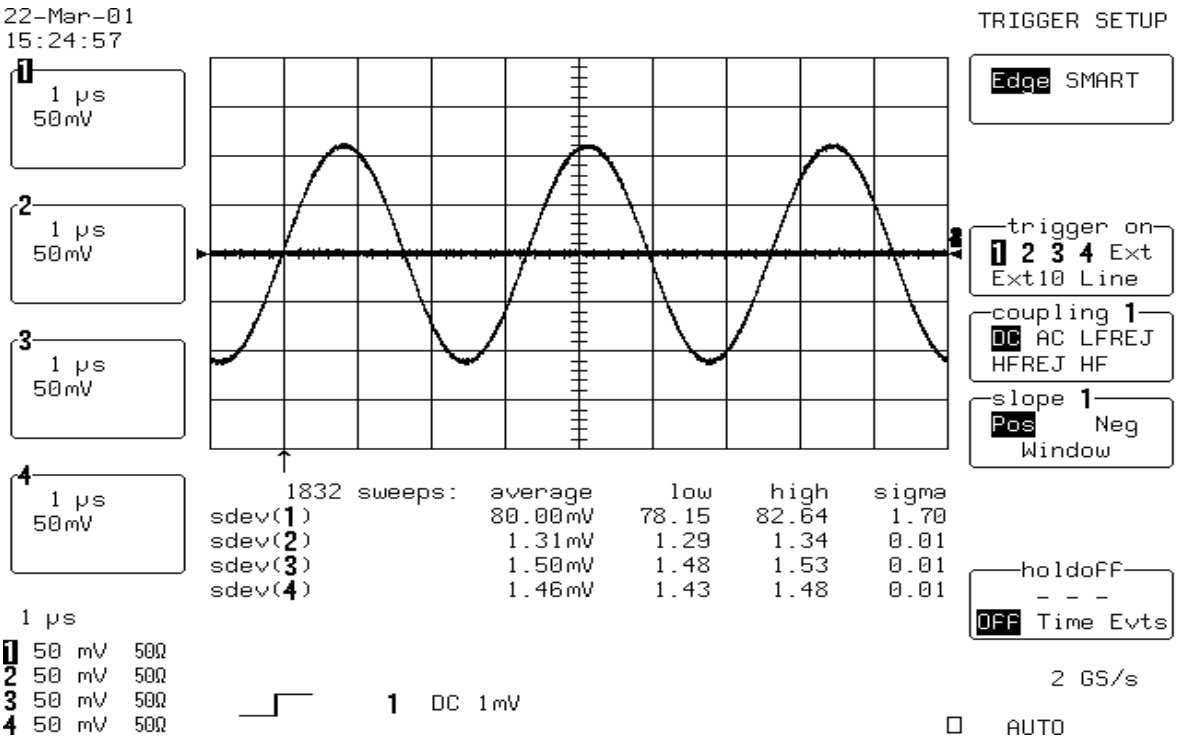
Figure 5-6 : 50Ω Bandwidth Equipment Setup

- Measure for at least 10 sweeps, record the average value of **sdev(1)** in Table 7 for LT37x or LT354 and Table 7A for LT26x.

- Repeat the above 3 steps for Channel 2, Channel 3 & Channel 4 substituting channel controls and input connector. Record the measurements in Table 7 for LT37x or LT354 and Table 7A for LT26x.

- Repeat the above measurement for all channels for 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz and 500.1 MHz and record the values in Table 7 for LT37X or LT354. For LT26X, use Table 7A for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 175.1 MHz & 350.1 MHz. For LT584, use Table 7B for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz, 500.1 MHz & 1000.1 MHz.

- Calculate the ratio to .3MHz for each frequency.
  Ratio = (sdev of XXXMHz) / (sdev of 0.3MHz)
  and compare the results to the limits in the test record.



▪ Recall **xxxP023.PNL** or configure the DSO as shown in 5.9 and for each Channel make the following change :

Input gain : **100mV/div**

- Connect the test equipment as shown in Figure 5-5.
- Set the generator frequency to **300 kHz**
- Set the generator amplitude to measure **0.800 mW** on the power meter.
- Read the displayed **generator output amplitude,** and record it in the third column of Table 8.
- Repeat the above measurement for 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz & 500.1 MHz. Record the generator output amplitude readout in the third column of Table 8 for LT37X or LT354. For LT26X, use Table 8A for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 175.1 MHz & 350.1 MHz. For LT584, use Table 7B for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz, 500.1 MHz & 1000.1 MHz.
- Disconnect the **RF output** of the HP8648B generator from the HP8482A power sensor.
- Connect the test equipment as shown in Figure 5-6.

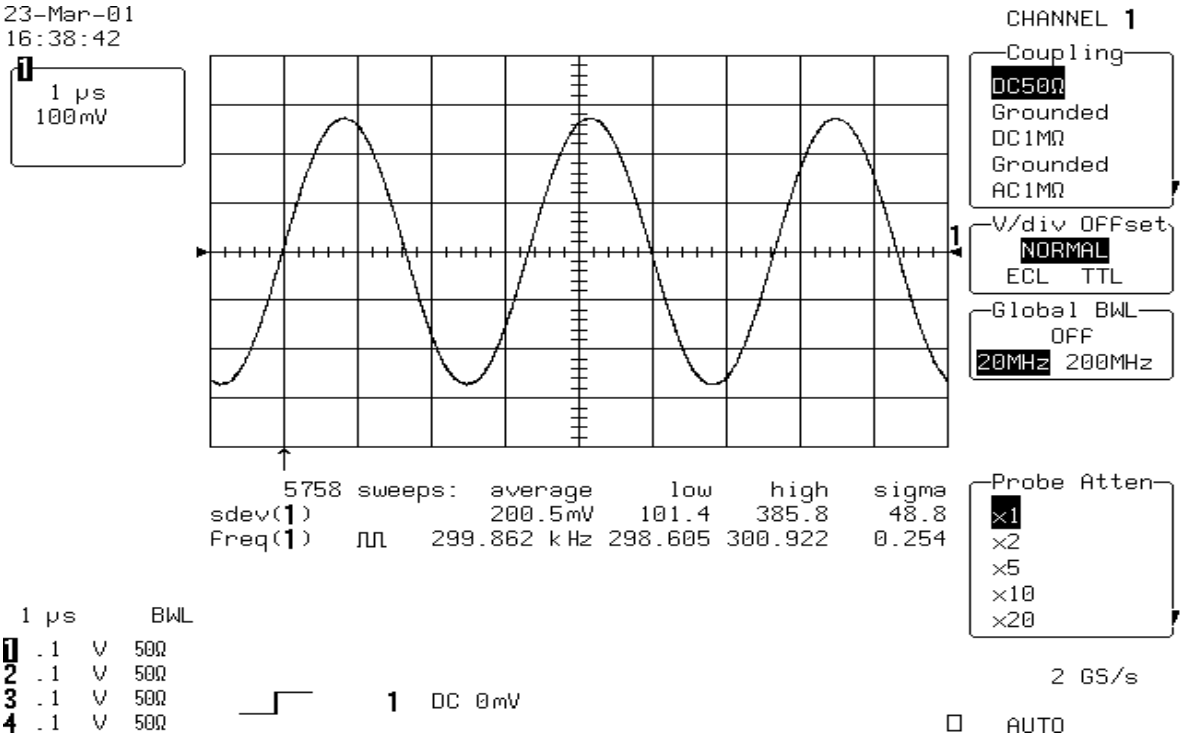
- Set the generator frequency to **300 kHz**.
- From the generator, apply the **recorded generator signal amplitude** to Channel 1.
- Press **Clear Sweeps**.
- Measure for at least 100 sweeps, record the average value of **sdev(1)** in Table 8 for LT37x or LT354, Table 8A for LT26x and Table 8B for LT584.
- Repeat the above 3 steps for Channel 2, Channel 3 & Channel 4 substituting channel controls and input connector. Record the measurements in Table 8 for LT37x or LT354, Table 8A for LT26x and Table 8B for LT584
- Repeat the above measurement for all channels for 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz and 500.1 MHz and record the values in Table 8 for LT37X or LT354. For LT26X, use Table 8A for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 175.1 MHz & 350.1 MHz. For LT584, use Table 8B for frequencies of 1.1 MHz, 10.1 MHz, 100.1 MHz, 250.1 MHz, 500.1 MHz & 1000.1 MHz.
- Calculate the ratio to .3 MHz for each frequency.
  Ratio = (sdev of XXXMHz) / (sdev of 0.3MHz)
  and compare the results to the limits in the test record.

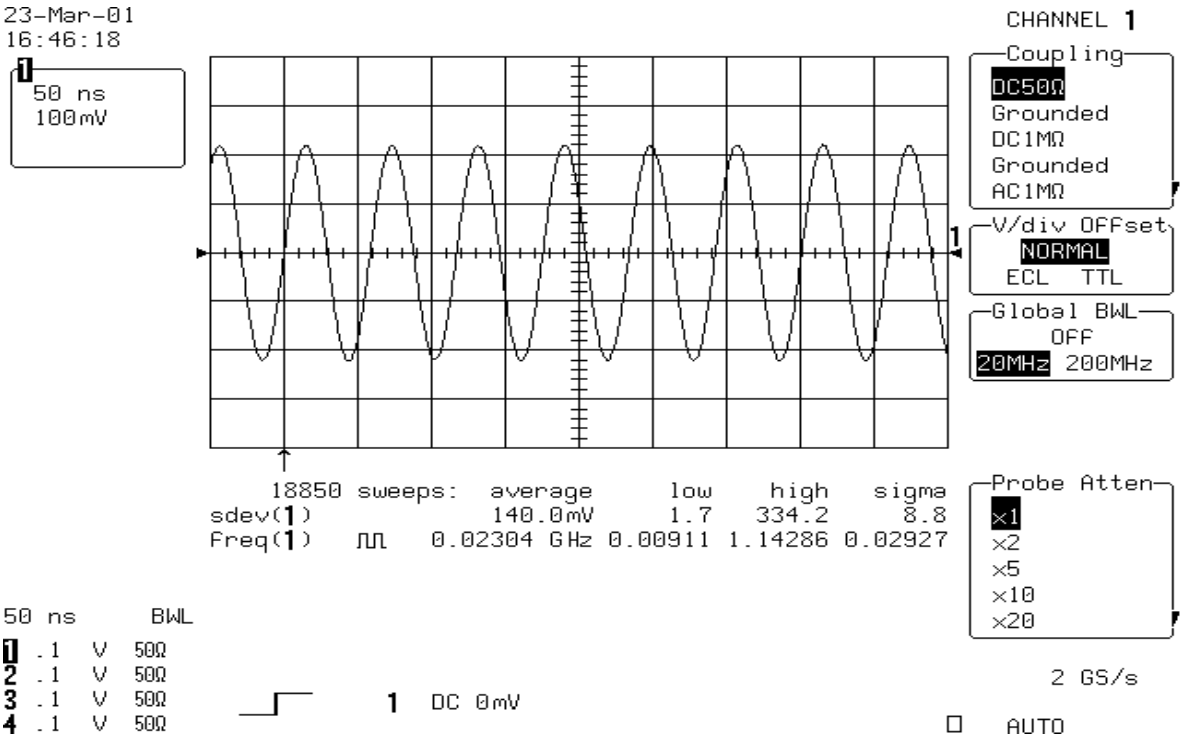
b. DC 50Ω with Bandwidth Limiter On

- Recall **xxxP024.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1**
Input Coupling	:	**DC 50Ω**
Global BWL	:	**20 MHz**
Input gain	:	**100 mV/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**1**
Slope line	:	**Pos**
Mode	:	**Auto**
Time base	:	**1 µsec/div**.
Channel use	:	**4**
Record up to	:	**25 k**
WAVE PILOT	:	**MEASURE**
Mode	:	**Custom**
Statistics	:	**Off**
Change parameters		
On line 1	:	**Sdev of 1**
On line 2	:	**Freq of 1**

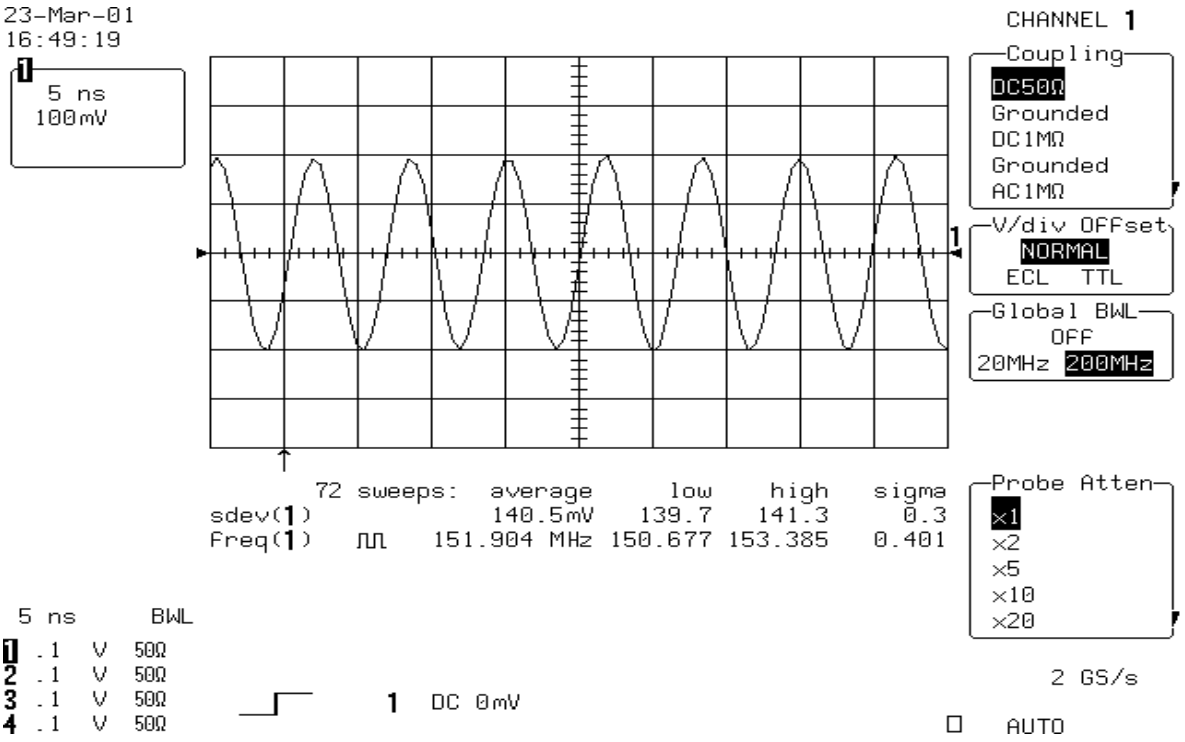
- Connect the test equipment as shown in Figure 5-6.
- Set the generator frequency to **300 kHz**.
- Adjust the generator signal amplitude to measure **sdev(1)** = **200 mV.**
- Set Time base : **50 nsec/div**.
- Increase the generator frequency until **sdev(1)** = **140 mV.** (typically 25 MHz)
- Press **Clear Sweeps**
- When **sdev(1)** = **140 mV,** record Freq(1) in Table 9.
- Check that the frequency is within the limits specified in Table 9.





- Set Global BWL : **200 MHz**
- Set Timebase : **5 nsec/div**.

- Increase the generator frequency until **sdev(1)** = **140 mV.** (typically 200 MHz)



- Press **Clear Sweeps**

- When **sdev(1)** = **140 mV,** record Freq(1) in Table 9.

- Repeat the 20 MHz and 200 MHz Bandwidth limiter tests for the other channels, substituting channel controls and input connector.

- Recall **xxxP025.PNL** for Channel 2**, xxxP026.PNL** for Channel3 **xxxP027.PNL** for Channel 4, or configure the DSO as shown in 5.9.1 Procedure and make the necessary changes.

- Record the test results in Table 9, and compare the results to the limits.

5.10 Trigger Level

The trigger capabilities are tested for several cases of the standard edge trigger:

- Channel (internal), and External Trigger sources
- Three DC levels: –3, 0, +3 major screen divisions
- DC coupling
- Positive and negative slopes

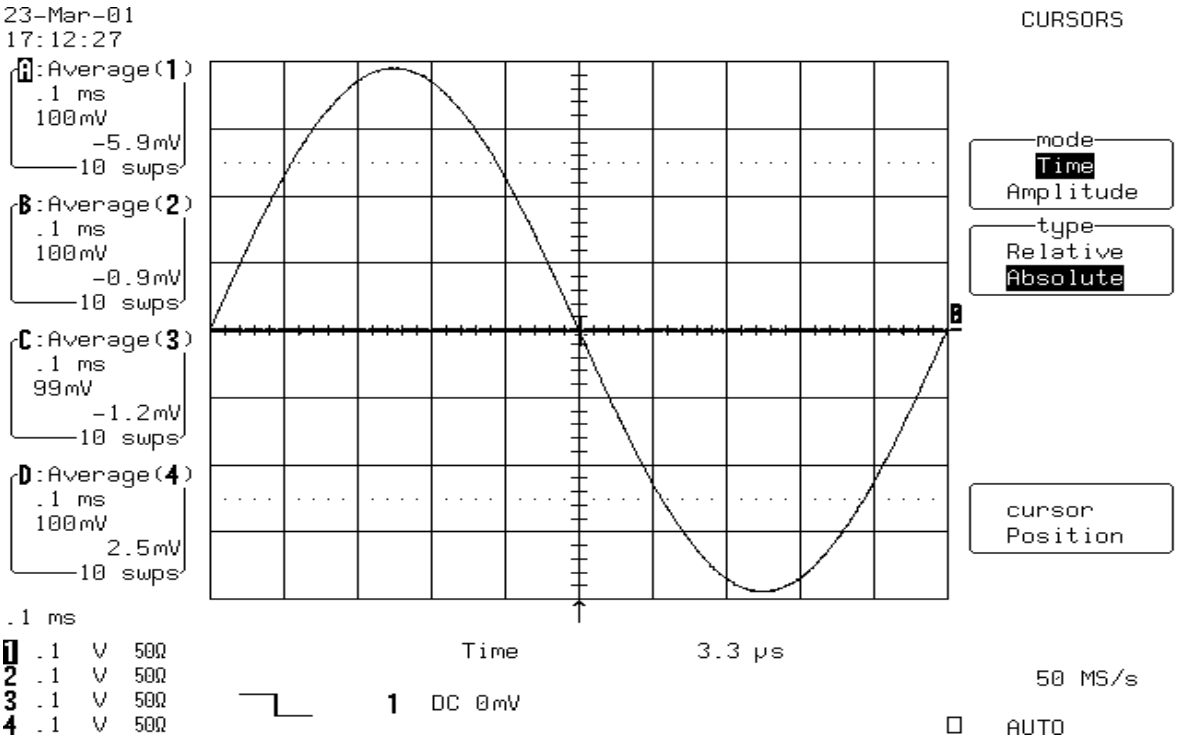
5.10.1 Channel Trigger at 0 Division Threshold

DC Coupling

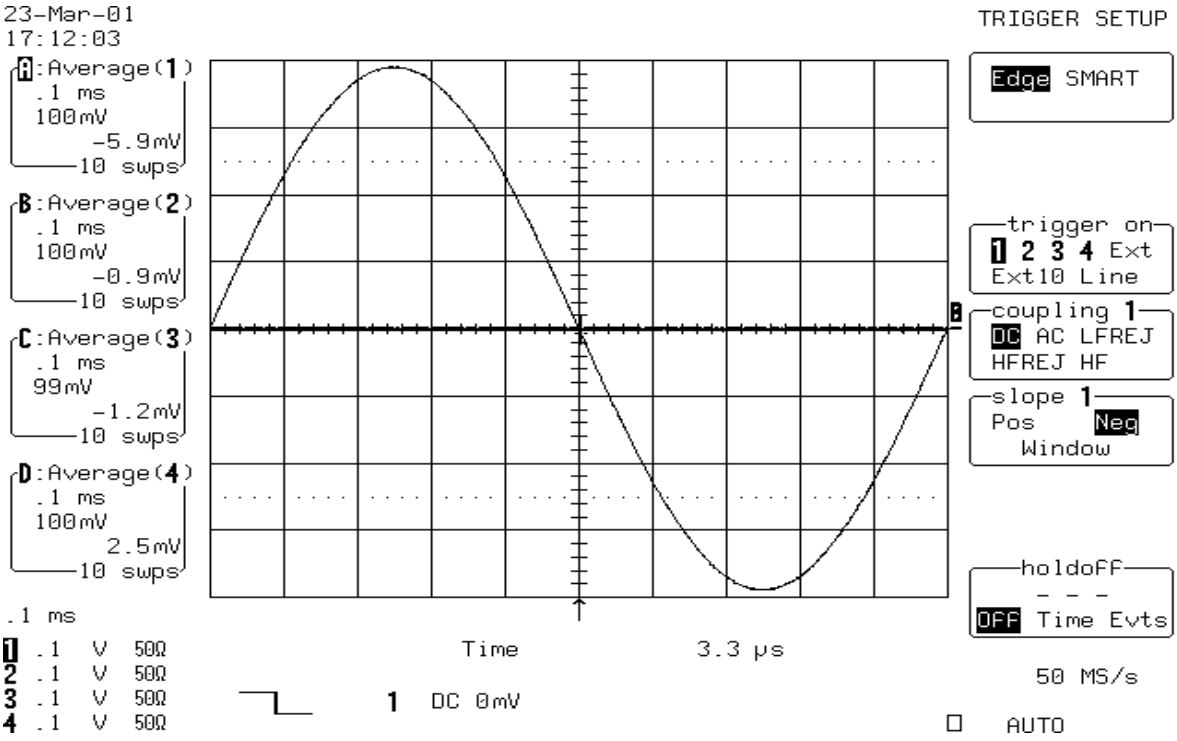
Recall **xxxP028.PNL** or configure the DSO:

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels Trace ON		**Channel 1, Channel 2, Channel 3 & Channel 4**
Input Coupling	:	**DC 50Ω** on all 4 Channels
Input gain	:	**100 mV/div.** on all 4 Channels
Input offset	:	**0 mV** on all 4 Channels (use show status to verify)
Trigger setup	:	**Edge**
Trigger on	:	**1**
Slope 1	:	**Pos**
Coupling	:	**DC**
Mode	:	**Auto**
Set Trigger level	:	**DC 0.0 mV**
Pre-Trigger Delay	:	**50 %**
Time base	:	**0.1 msec/div.**
Record up to	:	**50 k samples**
Channels Trace OFF		**Channel 1, Channel 2, Channel 3 & Channel 4**
ANALYSIS CONTROL		
Trace ON	:	**A, B, C & D**
Select Math TOOLS		
For Math	:	**Use at most 5000 points**
Redefine A, B, C, D		**Channel 1, Channel 2, Channel 3 & Channel 4**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**10 sweeps**

- Set the output of the LeCroy LW420 or equivalent audio frequency signal generator to **1 kHz.**
- Connect the output of the generator to Channel 1 through a 50 Ohm coaxial cable and adjust the sine wave output amplitude to get **8 divisions peak to peak .**
- Select WAVE PILOT : **Cursors, Time, Absolute**
- Use the "cursor position" knob, to move the **Time marker** at 0.0 µs



- Press **Clear Sweeps**,
- Acquire 10 sweeps and record in Table 10 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**
- Compare the test results to the corresponding limit in the test record.
- Set Trigger Slope 1 : **Neg**
- Acquire 10 sweeps and record in Table 10 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**



- Repeat steps 5.10.1.a. and 5.10.1.b. for all input channels, substituting channel controls (DC, Pos, Neg) and input connector.
  Recall **xxxP029.PNL** for Channel 2, **xxxP030.PNL** for Channel 3, **xxxP031.PNL** for Channel 4, or select **Trigger on** the Channel under test.
  The **Trigger level** is displayed in either the icon **2**, **3** or **4**

- Record the measurements in Table 10 and compare the test results to the corresponding limits in the test record.

5.10.2 Channel Trigger at +3 Divisions Threshold

DC Coupling

- Recall **xxxP032.PNL** or configure the DSO as shown in 5.10.1.a and for each Channel make the following change :

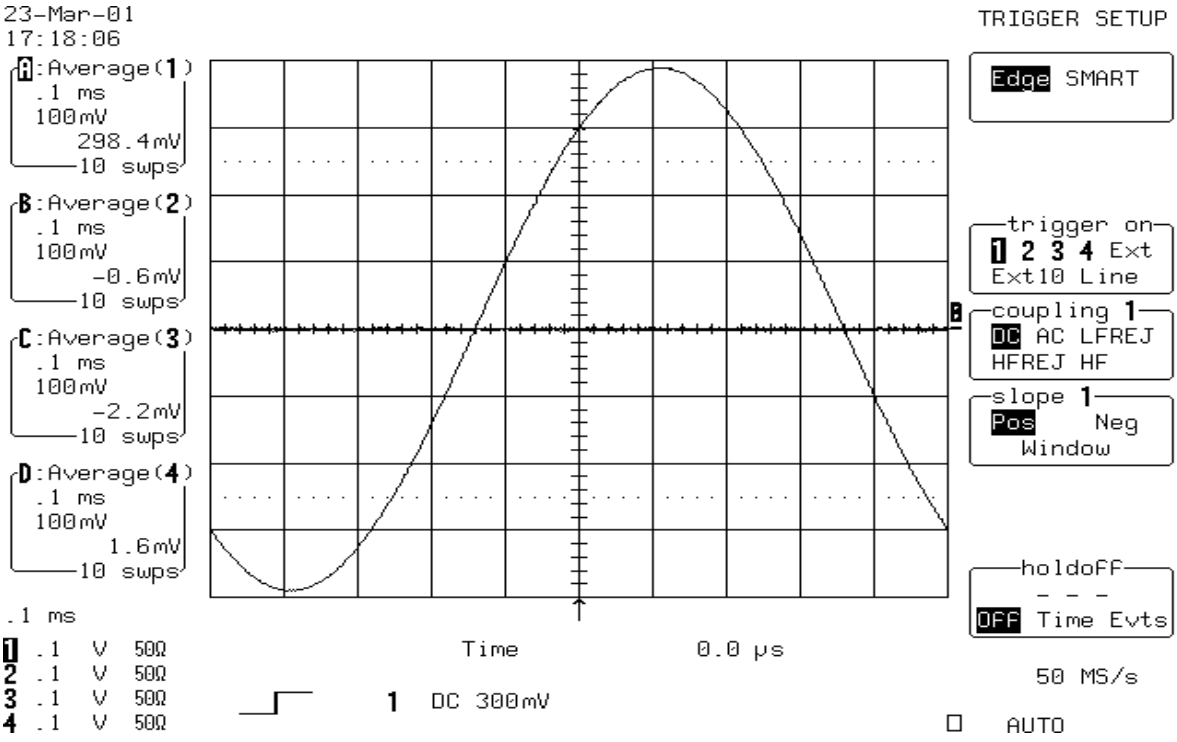
  Set Trigger level : **DC +300 mV**

- Connect the output of the generator to Channel 1 through a 50 Ohm coaxial cable.

- Press **Clear Sweeps**,

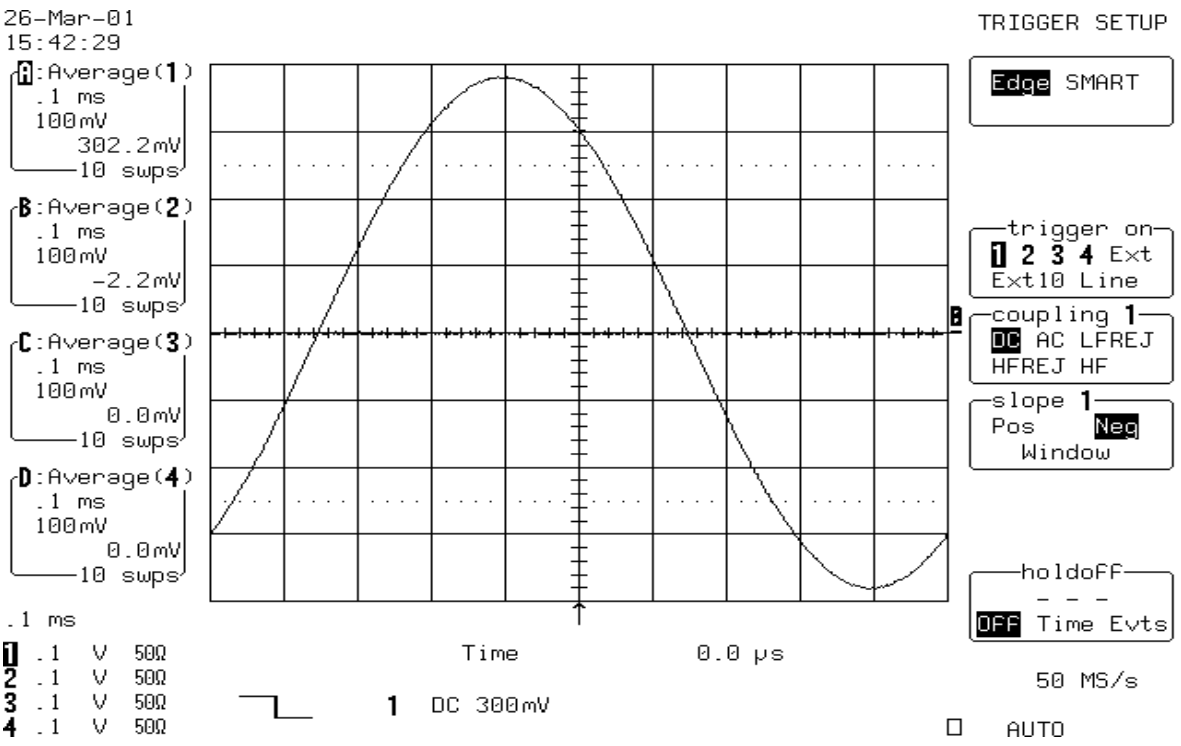
- Acquire 10 sweeps and record in Table 10 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**

- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope 1 : **Neg**

- Acquire 10 sweeps and record in Table 10 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**



- Repeat for all input channels, substituting channel controls (DC, Pos, Neg) and input connector. Recall **xxxP033.PNL** for Channel 2, **xxxP034.PNL** for Channel 3, **xxxP035.PNL** for Channel 4, or select **Trigger on** the Channel under test. The **Trigger level** is displayed in either the icon **2**, **3** or **4**

- Record the measurements in Table 10 and compare the test results to the corresponding limits in the test record.

5.10.3 Channel Trigger at –3 Divisions Threshold

DC Coupling

- Recall **xxxP036.PNL** or configure the DSO as shown in 5.10.1.a and for each channel make the following change :

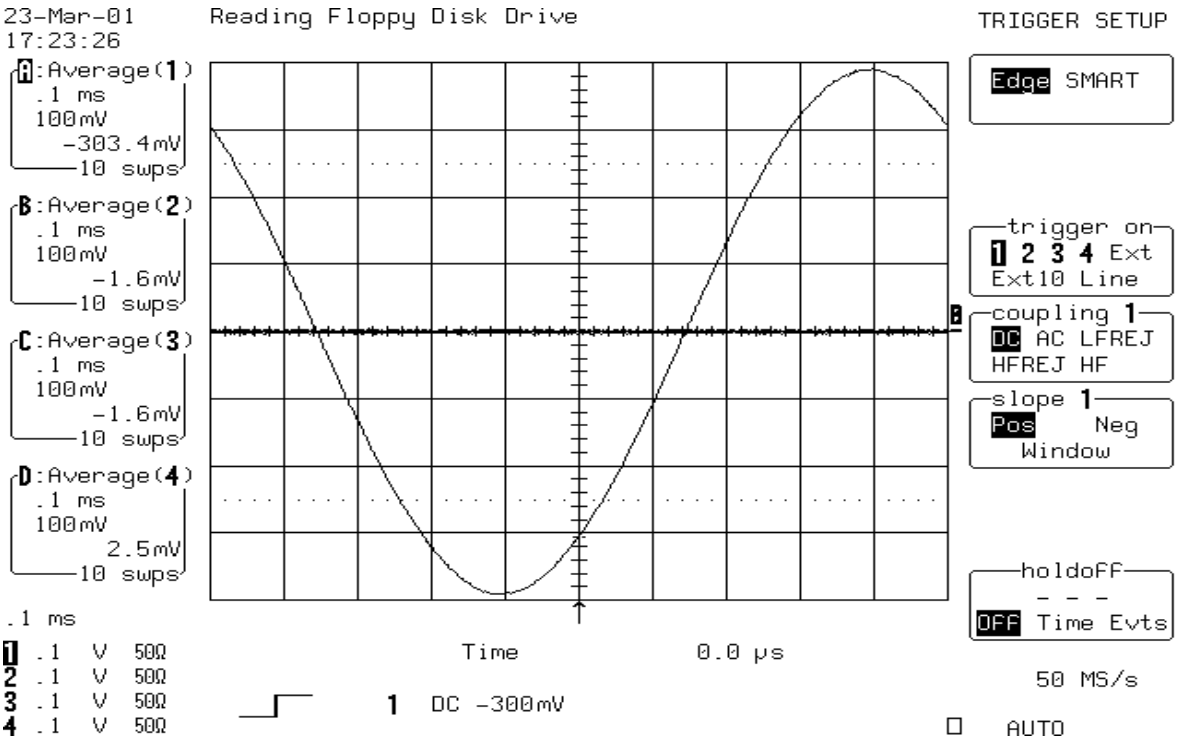
  Set Trigger level : **DC –300 mV**

- Connect the output of the generator to Channel 1 through a 50 Ohm coaxial cable.

- Press **Clear Sweeps**,

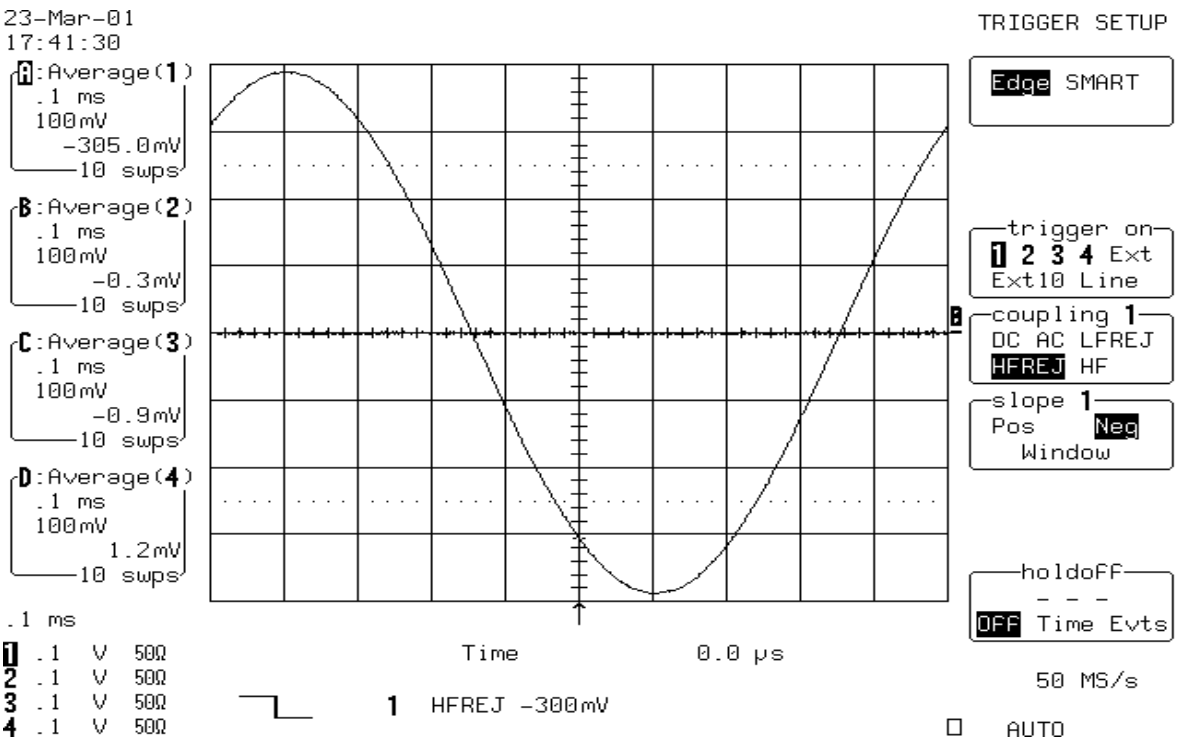
- Acquire 10 sweeps and record in Table 10 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**

- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope 1 : **Neg**

- Acquire 10 sweeps and record in Table 10 the **level** readout displayed below 100 mV in the icon **1,** at top left**.**



- Repeat for all input channels, substituting channel controls (DC, Pos, Neg) and input connector. Recall **xxxP037.PNL** for Channel 2, **xxxP038.PNL** for Channel 3, **xxxP039.PNL** for Channel 4, or select **Trigger on** the Channel under test. The **Trigger level** is displayed in either the icon **2**, **3** or **4**

- Record the measurements in Table 10 and compare the test results to the corresponding limits in the test record.

5.10.4 External Trigger at 0 Division Threshold

DC Coupling

- Recall **xxxP040.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channel Trace ON		**Channel 2**
Input Coupling	:	**DC 50Ω**
Input gain	:	**100 mV/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**Ext**
Slope Ext	:	**Pos**
Coupling Ext	:	**DC**
Set Trigger level	:	**0.0 mV**
External	:	**DC 1MΩ**
Mode	:	**Auto**
Pre-Trigger Delay	:	**50 %**
Time base	:	**0.1 msec/div.**
Record up to	:	**50 k samples**
Channel Trace OFF		**Channel 2**
ANALYSIS CONTROL		
Trace ON	:	**B**
Select Math TOOLS		
For Math	:	**Use at most 5000 points**
Redefine B	:	**Channel 2**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**10 sweeps**

- Connect the test equipment as shown in Figure 5-7.
- Set the output of the LeCroy LW420 or equivalent audio frequency signal generator to **1 kHz.**
- Adjust the sine wave output amplitude to get **8 divisions peak to peak .**
- Select WAVE PILOT : **Cursors, Time, Absolute**
- Use the "cursor position" knob, to move the **Time marker** at 0.0 µs

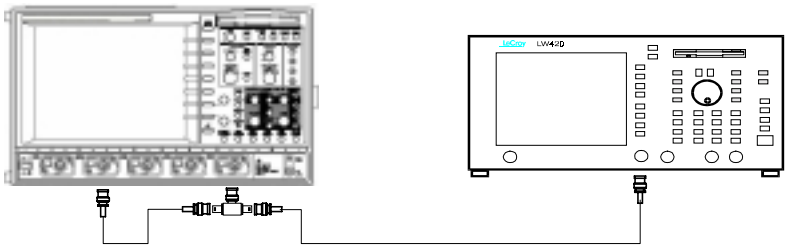
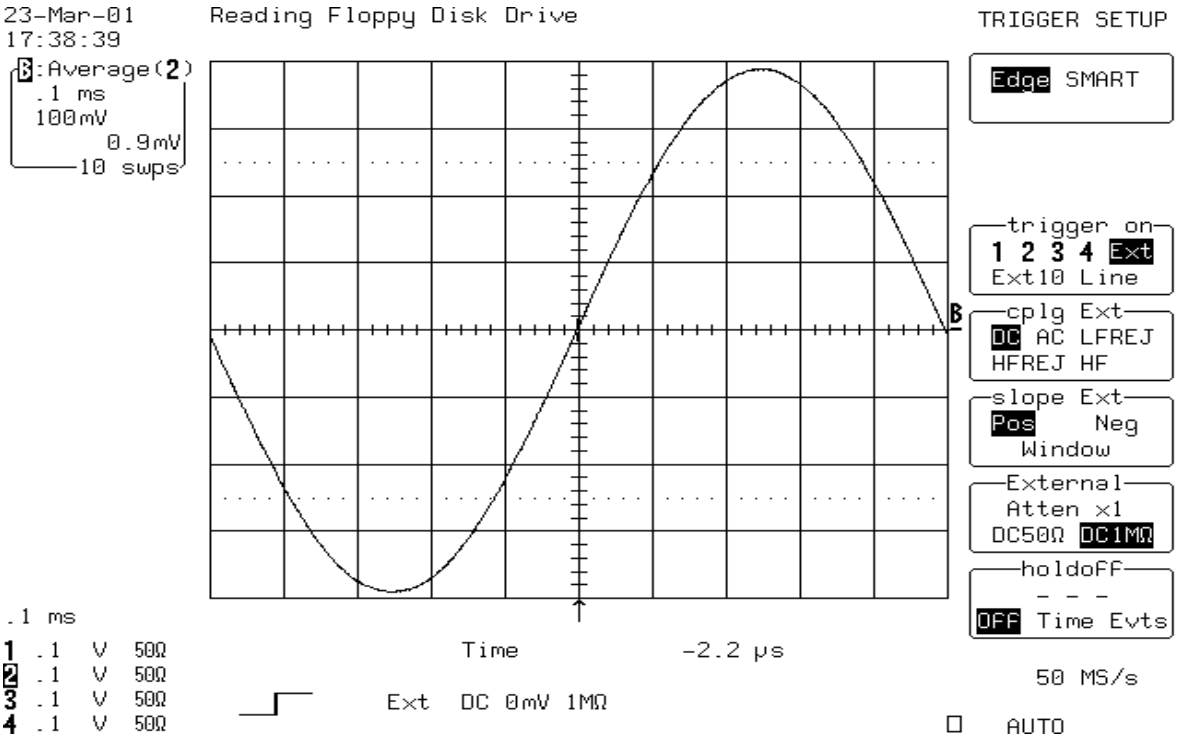


Figure 5-7 : External Trigger Equipment Setup

- Press **Clear Sweeps**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**



- Set Trigger Slope Ext : **Neg**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.

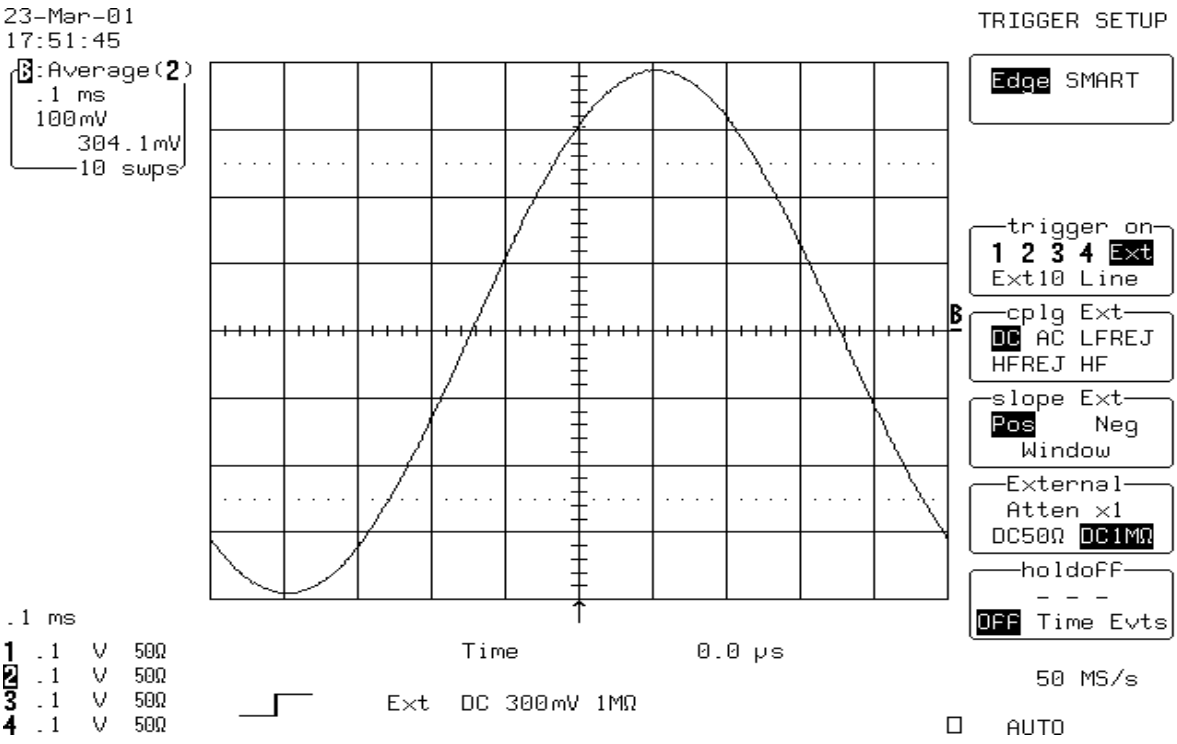
5.10.5 External Trigger at +3 Divisions Threshold

DC Coupling

- Recall **xxxP041.PNL** or configure the DSO as shown in 5.10.4.a and make the following change :

  Set Ext Trigger level : **DC +300 mV**

- Connect the test equipment as shown in Figure 5-7.
- Press **Clear Sweeps**,
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope Ext : **Neg**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

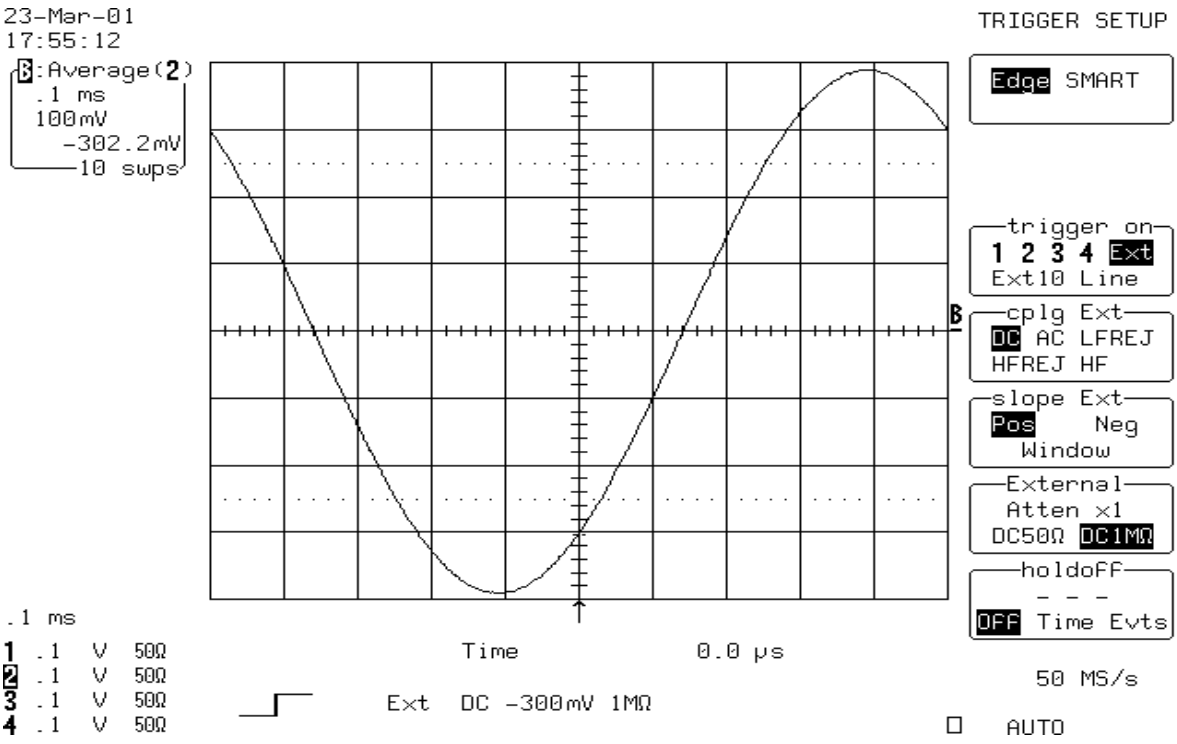
5.10.6 External Trigger at –3 Divisions Threshold

DC Coupling

- Recall **xxxP042.PNL** or configure the DSO as shown in 5.10.4.a and make the following change :

  Set Ext Trigger level : **DC –300 mV**

- Connect the test equipment as shown in Figure 5-7.
- Press **Clear Sweeps**.
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope Ext : **Neg**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

5.10.7 External/10 Trigger at 0 Division Threshold

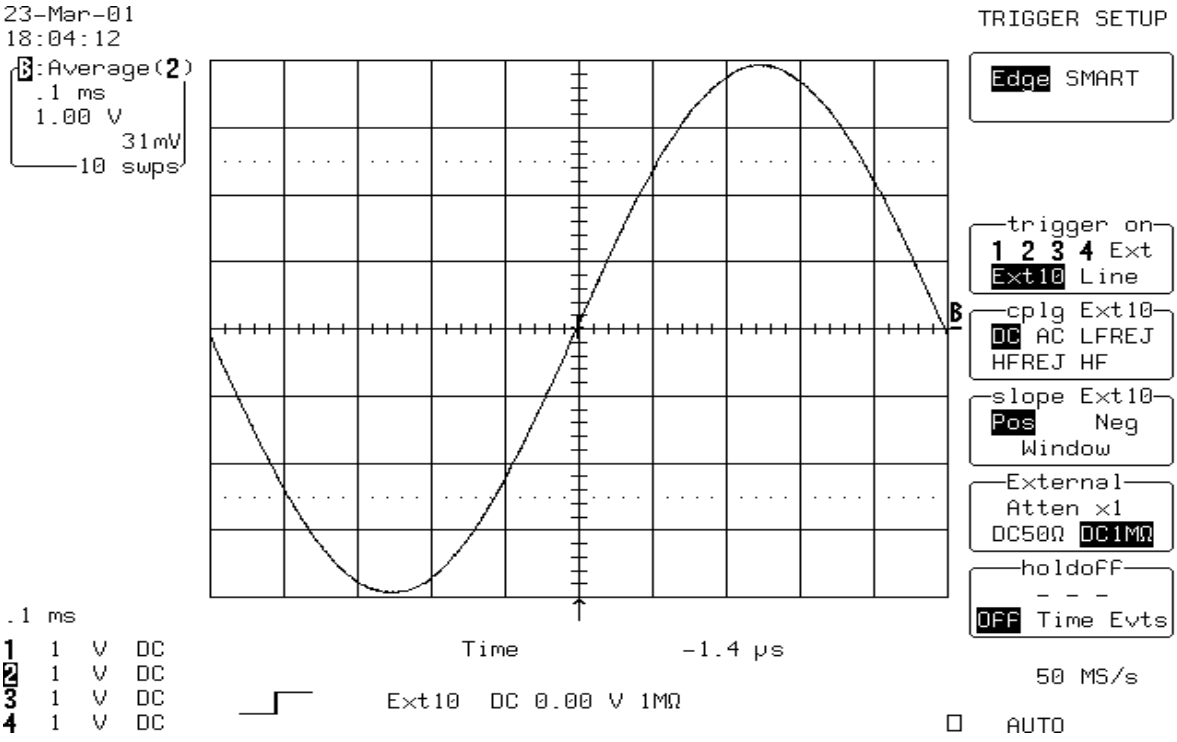
DC Coupling

- Recall **xxxP043.PNL** or configure the DSO :

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channel Trace ON		**Channel 2**
Input Coupling	:	**DC 1MΩ**
Input gain	:	**1V/div**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**Ext/10**
Slope Ext/10	:	**Pos**
Mode	:	**Auto**
Coupling	:	**DC**
Set Trigger level	:	**0.0 mV**
External	:	**DC 1MΩ**
Pre-Trigger Delay	:	**50 %**
Time base	:	**0.1 msec/div.**
Record up to	:	**50 k samples**
Channel Trace OFF		**Channel 2**
ANALYSIS CONTROL		
Trace ON	:	**B**
Select MATH TOOLS		
For Math	:	**Use at most 5000 points**
Redefine B	:	**Channel 2**
Use Math ?	:	**Yes**
Math Type	:	**Average**
Avg. Type	:	**Summed**
For	:	**10 sweeps**

- Connect the test equipment as shown in Figure 5-7.
- Set the output of the LeCroy LW420 or equivalent audio frequency signal generator to **1 kHz.**
- Adjust the sine wave output amplitude to get **8 divisions peak to peak .**
- Select WAVE PILOT : **Cursors, Time, Absolute**
- Use the "cursor position" knob, to move the **Time marker** at 0.0 μs
- Press **Clear Sweeps**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below

100 mV in the icon **2,** at top left**.**



- Set Trigger Slope Ext/10 : **Neg**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.

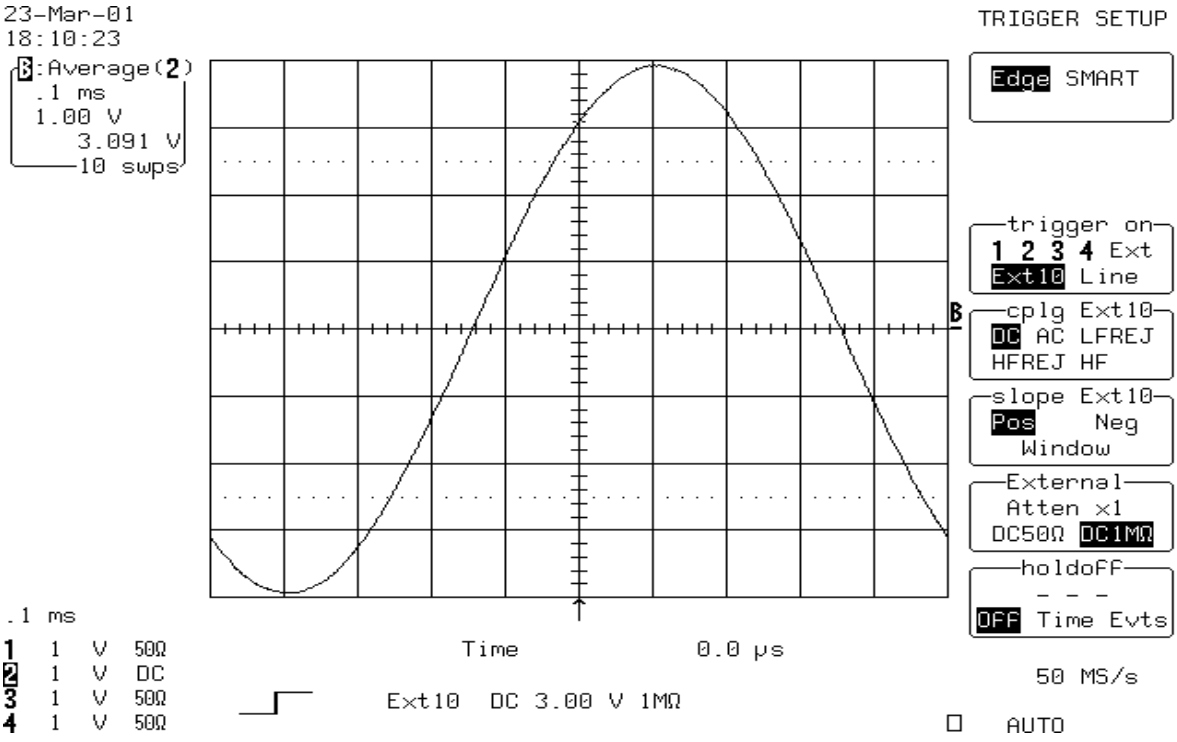
5.10.8 External/10 Trigger at +3 Divisions Threshold

DC Coupling

- Recall **xxxP044.PNL** or configure the DSO as shown in 5.10.7.a and make the following change :

  Set Ext/10 Trigger level : **DC +3 V**

- Connect the test equipment as shown in Figure 5-7.
- Press **Clear Sweeps**,
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope Ext/10 : **Neg**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

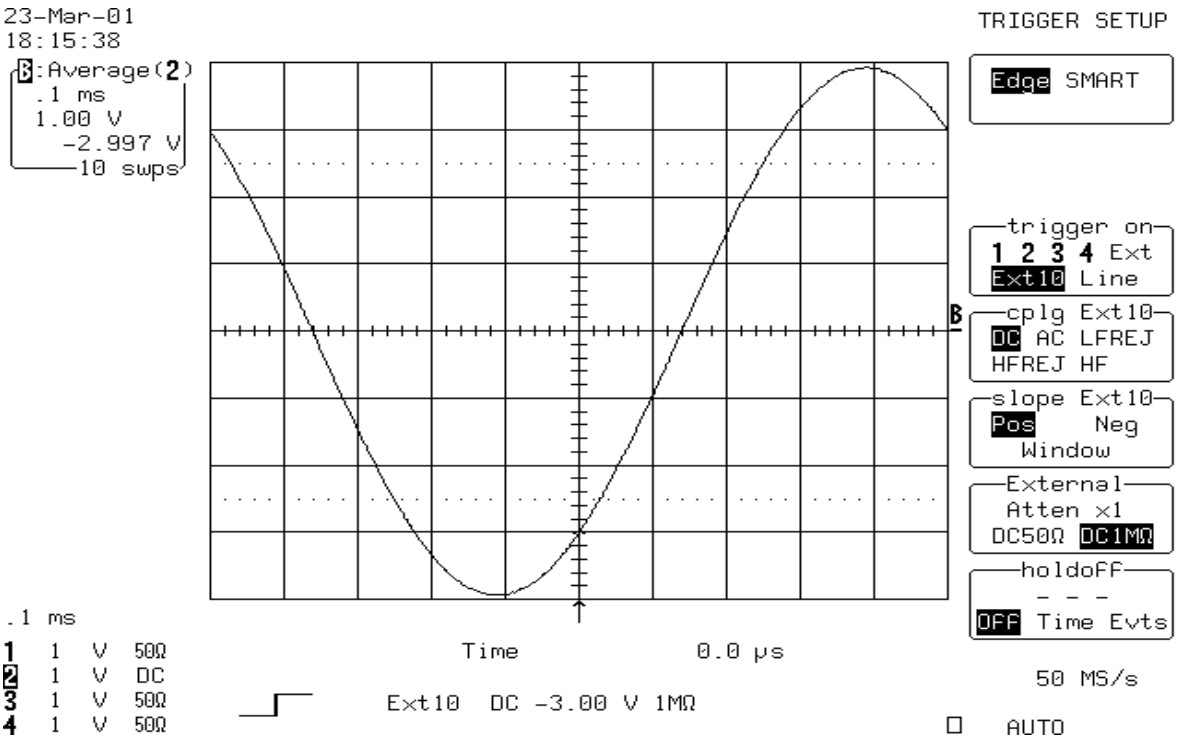
5.10.9 External/10 Trigger at –3 Divisions Threshold

DC Coupling

- Recall **xxxP045.PNL** or configure the DSO as shown in 5.10.7.a and make the following change :

  Set Ext/10 Trigger level : **DC –3 V**

- Connect the test equipment as shown in Figure 5-7.
- Press **Clear Sweeps**.
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**
- Compare the test results to the corresponding limit in the test record.



- Set Trigger Slope Ext/10 : **Neg**
- Acquire 10 sweeps and record in Table 11 the **level** readout displayed below 100 mV in the icon **2,** at top left**.**

5.11 Smart Trigger

5.11.1 Trigger on Pulse Width 10 nsec

a. Pulse Width < 10 nsec

- Recall **xxxP046.PNL** or configure the DSO

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels trace ON		**Channel 1**
Input coupling	:	**DC 50Ω**
Input gain	:	**.5 V/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Smart**
Setup Smart Trigger		**Glitch**
Trigger on	:	**1**
At the end of	:	**Neg.**
Width < 10 nsec	:	**On**
Width > 10 nsec	:	**Off**
Trigger mode	:	**Norm**
Time base	:	**5 nsec/div.**

- Connect the **RF output** of the HP8648B generator through a 5ns 50 Ohm BNC coaxial cable into Channel 1.

- Set the generator frequency to **100 MHz**. Adjust the generator output amplitude to get **5 divisions peak to peak .**

- Check that the scope Triggers. Record the test result in Table 12.

- Set Width < 10 nsec **Off** and Width > 10 nsec **ON**

- Check that the scope **doesn't trigger :** slow trigger and no flashes in box next to normal. Record the test result in Table 12.

b. Pulse Width > 10 nsec

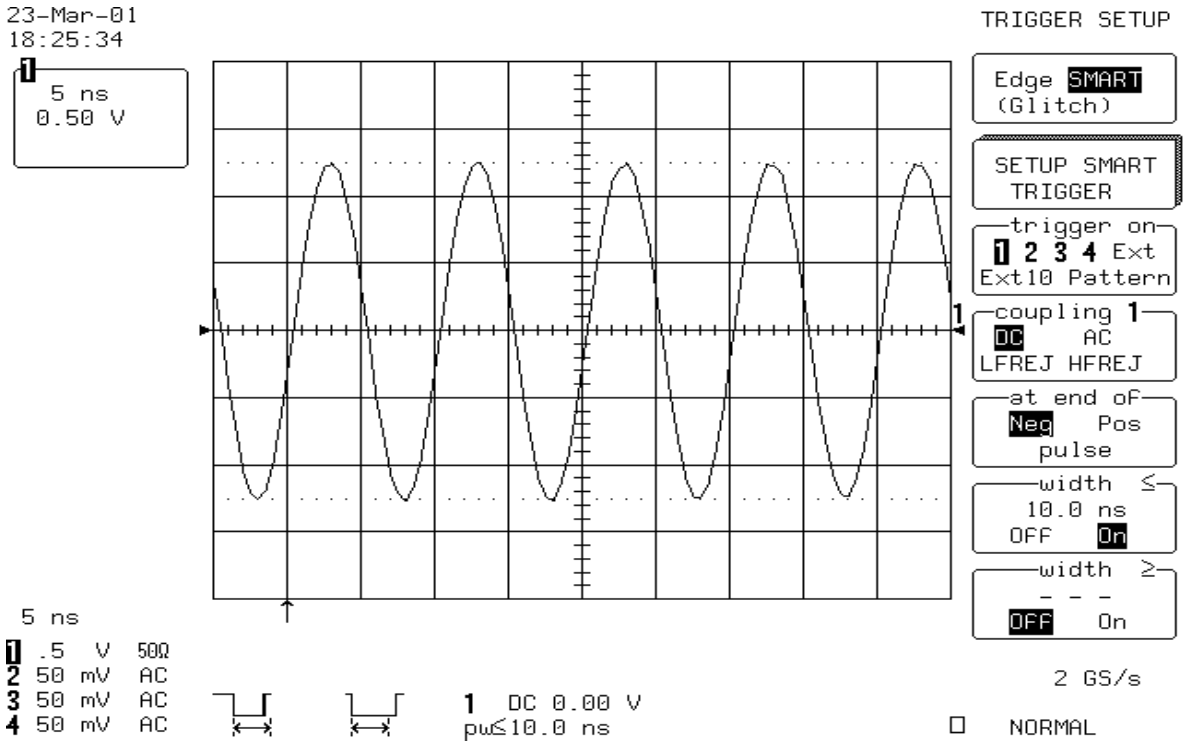
- Set the generator frequency to **40 MHz**.
- Set Width < 10 nsec **Off** and Width > 10 nsec **ON**

- Check that the scope Triggers. Record the test result in Table 12.

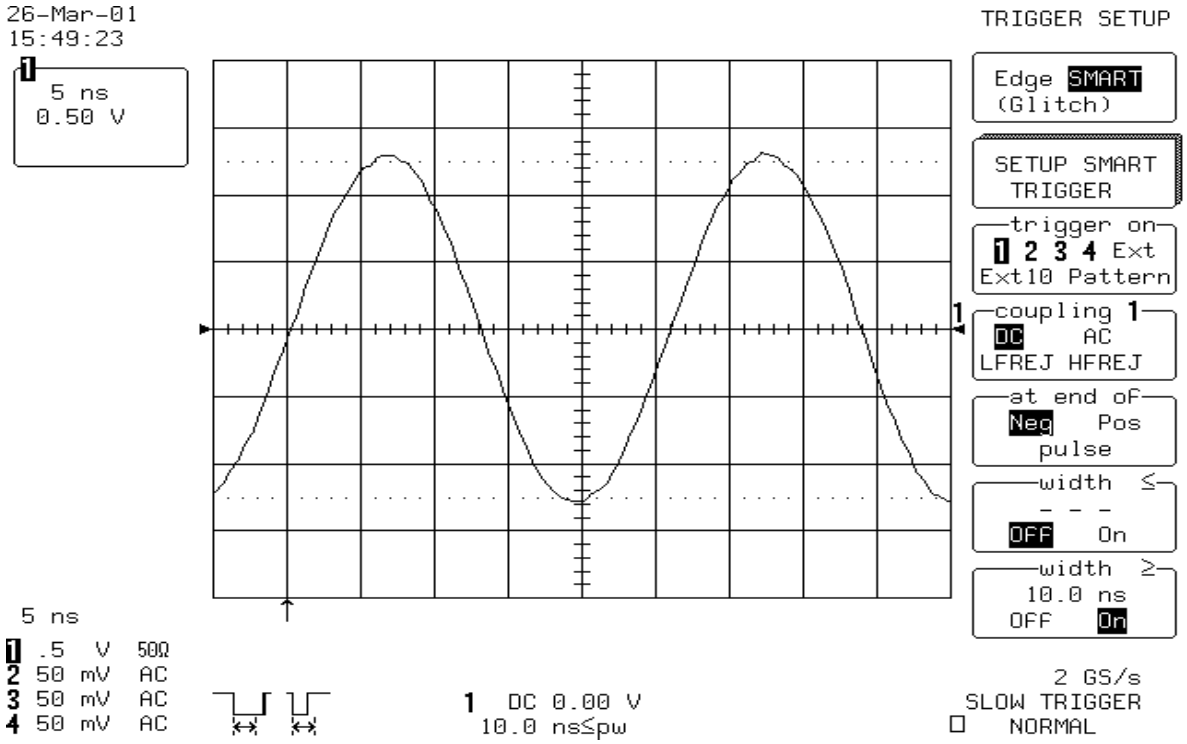
- Set Width < 10 nsec **On** and Width > 10 nsec **Off**

- Check that the scope **doesn't trigger :** slow trigger and no flashes in box. Record the test result in Table 12.

a. Pulse Width < 10 nsec



b. Pulse Width > 10 nsec



5.11.2 Trigger on Pulse Width 100 nsec

a. Pulse Width < 100 nsec

- Recall **xxxP047.PNL** or configure the DSO as shown in 5.11.1.a and make the following changes :

  Width < 100 nsec : **On**

  Width > 100 nsec **:** **Off**

  Time base : **20 nsec/div.**

- Set the generator frequency to **10 MHz**.

- Check that the scope Triggers. Record the test result in Table 12.

- Set Width < 100 nsec **Off** and Width > 100 nsec **ON**

- Check that the scope **doesn't trigger :** slow trigger and no flashes in box next to normal. Record the test result in Table 12.

b. Pulse Width > 100 nsec

- Set the generator frequency to **4 MHz**.

- Time base : **50 nsec/div.**

- Set Width < 100 nsec **Off** and Width > 100 nsec **ON**

- Check that the scope Triggers. Record the test result in Table 12.

- Set Width < 100 nsec **On** and Width > 100 nsec **Off**

- Check that the scope **doesn't trigger :** slow trigger and no flashes in box. Record the test result in Table 12.

5.12 Time Base Accuracy

An external sine wave generator of **0.1 MHz** with a frequency accuracy better than 1 PPM is used.

Specifications & Test limit

500 MHz clock : accuracy : **≤ ±0.001 % or ≤ ±10 PPM**

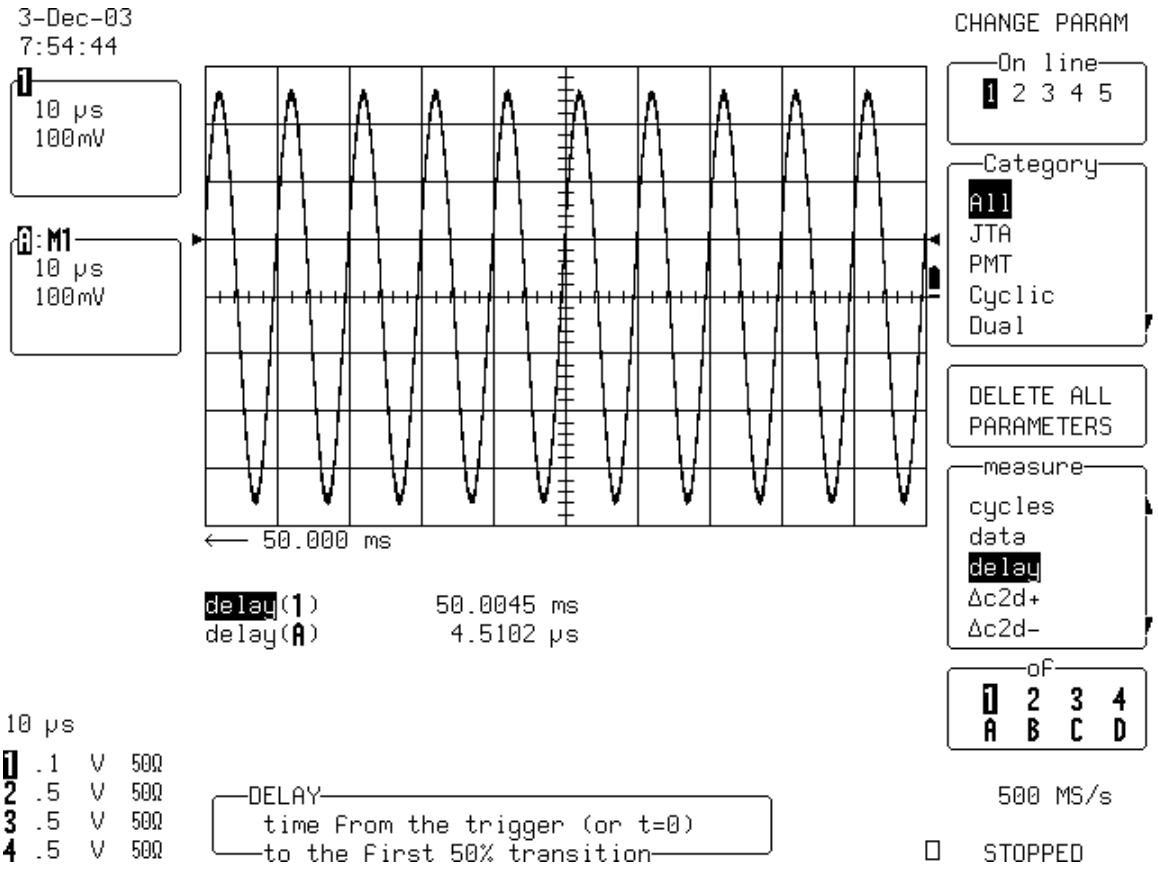
Procedure

- Recall **xxxP048.PNL** or configure the DSO

Panel Setups	:	**Recall FROM DEFAULT SETUP**
Channels trace ON		**Channel 1**
Input coupling	:	**DC 50Ω**
Input gain	:	**.1 V/div.**
Input offset	:	**0 mV**
Trigger setup	:	**Edge**
Trigger on	:	**1**
Coupling 1	:	**DC**
Slope 1	:	**Pos**
Level 1	:	**100 mV**
Trigger mode	:	**Norm**
Delay	:	**0 %**
Time base	:	**10 µsec/div.**
Channel use	:	**4**
Record up to	:	**50 k**

- Connect the **RF output** of the HP8648B generator through a 5ns 50 Ohm BNC coaxial cable into Channel 1.
- Set the generator frequency to **0.1 MHz**.
- Adjust the generator output amplitude to get **5 divisions peak to peak .**
- Store Channel 1 in Memory 1
- Recall **xxxP049.PNL** or make the following change :
- Set Post-trigger delay to **50.00 msec**
- Recall Memory **1 to A**
- Press : **WAVE PILOT**
- Measure : **MEASURE**
- Mode : **Custom**

- Statistics : **Off**
- Change parameters
- On line 1 : **Delay of 1**
- On line 2 : **Delay of A**
- Check that the displayed Channel 1 trace is **aligned** with the sine wave from memory 1.
- This allows the accuracy of the time base clock to be checked **5000 periods** after the trigger point. A difference of **±0.5 µsec** corresponds to **±10 PPM**.



- Calculate the Difference **{[delay(A) - delay(1)]+ 50 msec}.**
- Record the test result in Table 13, and compare it to the limit in the test record.

LeCroy Digital Storage Oscilloscope

Performance Certificate

LT584 & LT374/372 & LT354 & LT264/262 Manual Performance Test Procedure
Version D – December 2003

Model_____ Serial Number_____ Customer_____

Software Version_____

Inspection Date_____ Next Due_____

Temperature_____ Humidity_____%

Tested By_____ Report Number_____

Place of Inspection_____

Condition found_____ Condition Left_____

Approved By_____

Test Equipment Used

Instrument	Model	S/N	Cal Due Date
Signal Generator Radio Frequency	_____	_____	_____
Signal Generator Audio Frequency	_____	_____	_____
Voltage Generator DC Power Supply	_____	_____	_____
Step Generator Fast Pulser	_____	_____	_____
Digital Multimeter Voltmeter, Ohmmeter	_____	_____	_____

Traceable to_____

Table 1: LT584 & LT374/372 & LT354 & LT264/262 Test Report

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Coupling	Volts/div.	Measured Channel 1 Impedance Ω, MΩ	Measured Channel 2 Impedance Ω, MΩ	Measured Channel 3 Impedance Ω, MΩ	Measured Channel 4 Impedance Ω, MΩ	Measured External Impedance Ω, MΩ	Measured External/10 Impedance Ω, MΩ	Lower Limit Ω, MΩ	Upper Limit Ω, MΩ
DC 1MΩ	50 mV/div							0.99 MΩ	1.01 MΩ
DC 1MΩ	200 mV/div					N/A	N/A	0.99 MΩ	1.01 MΩ
AC 1MΩ	50 mV/div					N/A	N/A	1.188 MΩ	1.212 MΩ
AC 1MΩ	200 mV/div					N/A	N/A	0.99 MΩ	1.01 MΩ
DC 50Ω	50 mV/div						N/A	49.5 Ω	50.5 Ω
DC 50Ω	200 mV/div					N/A	N/A	49.5 Ω	50.5 Ω

Table 2: Impedance Test Record

Coupling	Volts/div.	Measured Channel 1 Leakage mV	Measured Channel 2 Leakage mV	Measured Channel 3 Leakage mV	Measured Channel 4 Leakage mV	Measured External Leakage mV	Lower Limit mV	Upper Limit mV
DC 1MΩ	50 mV/div						–1	+1
DC 1MΩ	200 mV/div						–1	+1

Table 3: Leakage Current Test Record

Coupling	Time/Div.	Measured sdev Channel 1 mV	Measured sdev Channel 2 mV	Measured sdev Channel 3 mV	Measured sdev Channel 4 mV	LT37x	LT354 LT26x
						Limits mV	
DC 1MΩ	20 ms					0.5	0.45
DC 1MΩ	1 ms					0.5	0.45
DC 1MΩ	50 µs					0.5	0.45
DC 1MΩ	2 µs					0.5	0.45
AC 1MΩ	2 µs					0.5	0.45
DC 50Ω	2 µs					0.5	0.45
DC 50Ω	20 µs					0.5	0.45

Table 4: RMS Noise Test Record

Volts /div	Attenuator	P S Out Put	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
			DMM 1	Mean (A)	Δ 1 Mean– DMM	DMM 2	Mean (B)	Δ 2 Mean– DMM	DMM 3	Mean (C)	Δ 3 Mean– DMM	DMM 4	Mean (D)	Δ 4 Mean– DMM	
2 mV	X 100 40 db	+0.6 V													±1.25mV
		-0.6V													±1.25mV
5 mV	X 100 40 db	+1.5 V													±1.625 mV
		-1.5V													±1.625 mV
10 mV	X 100 40 db	+3.0 V													±2.25 mV
		-3.0V													±2.25 mV
20 mV	X 100 40 db	+6.0 V													±2.5 mV
		-6.0V													±2.5 mV
50 mV	X 10 20 db	+1.5V													±7.25mV
		-1.5V													±7.25mV
0.1 V	X 10 20 db	+3.0 V													±13.5mV
		-3.0V													±13.5mV
1 V	X 1	+3.0 V													±126mV
		-3.0V													±126mV
5 V	X 1	+15V													±0.626V
		-15V													±0.626V

Table 5: DC Accuracy Test Record

Volt /div.	Coupling DC	DSO offset	P S output	Measured Channel 1 V & mV			Measured Channel 2 V & mV			Measured Channel 3 V & mV			Measured Channel 4 V & mV			Limits
				DMM 1	Mean (A)	Δ 1 Mean– DMM	DMM 2	Mean (B)	Δ 2 Mean– DMM	DMM 3	Mean (C)	Δ 3 Mean– DMM	DMM 4	Mean (D)	Δ 4 Mean– DMM	mV
5mV	1 MΩ	+1 V	–1 V													±16.2
5mV	1 MΩ	-1 V	+1 V													±16.2
5mV	1MΩ	0V	0V													±1.2

Table 6: Offset Test Record

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	mW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.200			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.200										0.91	1.09
10.1	0.200										0.91	1.09
100.1	0.200										0.91	1.09
250.1	0.200										0.86	1.12
500.1	0.200										0.73	1.11

Table 7: DC 50Ω, 50 mV/div. Bandwidth Test Record for LT37x and LT354

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	mW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.200			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.200										0.91	1.09
10.1	0.200										0.91	1.09
100.1	0.200										0.91	1.09
175.1	0.200										0.86	1.12
350.1	0.200										0.73	1.11

Table 7A: DC 50Ω, 50 mV/div. Bandwidth Test Record for LT26x

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	mW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.200			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.200										0.91	1.09
10.1	0.200										0.91	1.09
100.1	0.200										0.91	1.09
250.1	0.200										0.86	1.12
500.1	0.200										0.81	1.12
1000.1	0.200										0.73	1.11

Table 7B: DC 50Ω, 50 mV/div. Bandwidth Test Record for LT584

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	mW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.800			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.800										0.91	1.09
10.1	0.800										0.91	1.09
100.1	0.800										0.91	1.09
250.1	0.800										0.86	1.12
500.1	0.800										0.73	1.11

Table 8: DC 50Ω, 100 mV/div. Bandwidth Test Record for LT37x and LT354

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	mW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.800			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.800										0.91	1.09
10.1	0.800										0.91	1.09
100.1	0.800										0.91	1.09
175.1	0.800										0.86	1.12
350.1	0.800										0.73	1.11

Table 8A: DC 50Ω, 100 mV/div. Bandwidth Test Record for LT26x

Frequency	Measured Power	Generator Amplitude	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		Lower Limit	Upper Limit
MHz	MW	mV	Sdev(1) mV	Ratio(1) to 0.3	Sdev(2) mV	Ratio(2) to 0.3	Sdev(3) mV	Ratio(3) to 0.3	Sdev(4) mV	Ratio(4) to 0.3		
0.300	0.800			N/A		N/A		N/A		N/A	N/A	N/A
1.1	0.800										0.91	1.09
10.1	0.800										0.91	1.09
100.1	0.800										0.91	1.09
250.1	0.800										0.86	1.12
500.1	0.800										0.81	1.12
1000.1	0.800										0.73	1.11

Table 8B: DC 50Ω, 100 mV/div. Bandwidth Test Record for LT584

Global BWL	Amplitude at 300 kHz	Measured Channel 1		Measured Channel 2		Measured Channel 3		Measured Channel 4		LT37x LT354		LT26x	
										Lower Limit	Upper Limit	Lower Limit	Upper Limit
MHz	Sdev mV	Sdev(1) mV	Freq(1) MHz	Sdev(2) mV	Freq(2) MHz	Sdev(3) mV	Freq(3) MHz	Sdev(4) mV	Freq(4) MHz	MHz	MHz	MHz	MHz
20	200	140		140		140		140		10	37	10	37
200	200	140		140		140		140		110	290	110	280

Table 9: DC 50Ω, Bandwidth Limiter Test Record

Trigger Level	Trigger Slope	Channel 1	Channel 2	Channel 3	Channel 4	Lower Limit	Upper Limit
mV		Measured DC Trigger Level (1) mV	Measured DC Trigger Level (2) mV	Measured DC Trigger Level (3) mV	Measured DC Trigger Level (4) mV	mV	mV
0	Pos					–30	+30
0	Neg					–30	+30
+300	Pos					+270	+330
+300	Neg					+270	+330
–300	Pos					–270	–330
–300	Neg					–270	–330

Table 10: Channel DC Trigger Test Record

Trigger Slope	External Trigger Level	External DC	External Limits		External/10 Trigger Level	External/10 DC	External/10 Limits	
	mV	Measured DC Trigger Level (Ext) mV	Lower MV	Upper mV	V	Measured DC Trigger Level (Ext10) V	Lower V	Upper V
Pos	0		–50	+50	0		–0.5	+0.5
Neg	0		–50	+50	0		–0.5	+0.5
Pos	+300		+250	+350	+3		+2.5	+3.5
Neg	+300		+250	+350	+3		+2.5	+3.5
Pos	–300		–250	–350	–3		–2.5	–3.5
Neg	–300		–250	–350	–3		–2.5	–3.5

Table 11: External & Ext/10 DC Trigger Test Record

Smart Trigger Pulse Width ns	Generator Frequency MHz	Width <	Width >	Triggered	Pass
< 10	100	On	Off	Yes	
< 10	100	Off	On	No	
> 10	40	Off	On	Yes	
> 10	40	On	Off	No	
< 100	10	On	Off	Yes	
< 100	10	Off	On	No	
> 100	4	Off	On	Yes	
> 100	4	On	Off	No	

Table 12: Smart Trigger Test Record

Generator Frequency MHz	Post Trigger Delay Msec	Delay (A) µs	Delay (1) msec	Difference delay(A) – delay(1)+50msec	Lower Limit µsec	Upper Limit µsec
0.1000	50.0				-0.5	+0.5

Table 13: Time Base Test Record

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6. Maintenance

6.1 Introduction

This section contains information necessary to maintain, calibrate and troubleshoot the LeCroy waverunner digital storage oscilloscopes.

6.1.1 Safety Precautions

The  symbol used in this manual indicates dangers that could result in personal injury.

The  symbol used in this manual identify conditions or practices that could damage the instrument.

 The following servicing instructions are for use by qualified personnel only. Do not perform any servicing other than contained in service instructions. Refer to procedures prior to performing any service.

 Exercise extreme safety when testing high energy power circuits. Always turn the power OFF, disconnect the power cord, discharge the cathode ray tube and all capacitors before disassembling the instrument.

6.1.2 Antistatic Precautions

 Any static charge that builds on your person or clothing may be sufficient to destroy CMOS components, integrated circuits, Gate array's.....etc.

In order to avoid possible damage, the usual precautions against static electricity are required.

- Handle the boards in antistatic boxes or containers with foam specially designed to prevent static build-up.
- Ground yourself with a suitable wrist strap.
- Disassemble the instrument at a properly grounded work station equipped with antistatic mat.
- When handling the boards, do not touch the pins.
- Stock the boards in antistatic bags.

6.2 Software Update Procedure

6.2.1 Upgrading Firmware

LeCroy Corporation has a policy of continually improving and upgrading its products.

The LT Series instrument is equipped with flash Prom on processor board.
The software is updated to the latest version using either the floppy disk drive or the memory card interface.

After any software change, reboot the scope or perform a general reset of the instrument by simultaneously depressing the F2 button, the F5 menu button and the CH1 button.

a. Performing the Update from Floppy

- Format a single high density 1.44Mb floppy in the scope (not in the PC)
- Create a directory LECROY_P in the root directory of the disk
- Copy the file VXFOUND.FLA, into the directory created above.
- Label this disk " Firmware Update Disk "
- Cycle power to the scope with no floppy inserted.
- When the scope boots enter the "Show Status" , "System" menu to verify that version 08.1.1 or later is currently running.
- Insert the Firmware Update Disk into the scope's floppy drive.
- Select "Utilities", "Special Modes", "Firmware Update", "Update from Floppy" .
- Press twice "Update Flash".
- Wait for two minutes until displaying "FLASH UPDATE SUCCESSFUL"on the DSO.
- When the operation is complete remove the floppy and reboot the scope.
- When the scope boots enter the "Show Status", "System " menu to verify that the new version is currently running.

Warning:

Reprograming the Flash memory is a procedure to be perform with care.
Any loss of power during the update process could cause the scope to require Factory service.
Note that once software has update it is not possible to revert to the previous software version.

b. Performing the Update from Card

- Format a 2Mb SRAM memory card
- Create a directory LECROY_P in the root directory of the card
- Copy the file VXFOUND.FLA, into the directory created above.
- Cycle power to the scope with no floppy or card inserted.

- When the scope boots enter the “Show Status“ , “System“ menu to verify that version 8.1.1 or later is running.
- Insert the Card created above into the PCMCIA Slot.
- Select “Utilities“, “Special Modes“, “Firmware Update“, “Update from Card“ .
- Press twice “Update Flash“.
- Wait for two minutes until displaying “FLASH UPDATE SUCCESSFUL”on the DSO.
- When the operation is complete remove the card and reboot the scope.
- When the scope boots enter the “Show Status“, “System “ menu to verify that the new version is currently running.

6.2.2 Software Options

The following software options are available:

- EMM Extended Math & Measurement
- WAVA Wave Analysis
- MC01 PCMCIA Memory Card
- JTA Jitter and Timing Analysis

6.2.2.1 Changing Software Option Key

a. Scope ID, Scope Serial Number

The scope ID and scope s/n: are used to request a Software Option Key

- Enter the scope's Software Options menu (located under the **STATUS**, **SYSTEM** menu).
- Note the **SCOPEID**, i.e: C63B9B-A5 and **Scope s/n**: LT34400156 that are found on that menu.

b. Entering Option Key in the DSO

- Enter the scope's Software Options menu (**STATUS**, **SYSTEM** menu).
- Enter the **ADD OPTION KEY** menu on the DSO
- Enter the new option key using the dymo-editor, i.e: **C4B5-F4A9-4464-E7ED**
- Click on **ENTER THIS OPTION KEY** to add the key
- Reboot the scope and verify that the options added correctly.

Then check in the system summary, by using the show status button on the front panel, the scope serial number.

6.3 Equipment and Spare Parts Recommended for Service

6.3.1 Test Equipment Required

See Table 5-1 in section 5.2.

6.3.2 LT Series Spare Parts

Parts Number	Assembly	Adjustments or Confirmations	Performance Tests
213025610	CPU Board without DRAM	6.4.1	None
213025605	Main Board for LT344/344L without HMM436's	6.4.2	None
213025650	Main Board for LT342/342L without HMM436's	6.4.2	None
213025648	Main Board for LT322 without HMM436's	6.4.2	None
213025670	Main Board for LT224 without HMM436's	6.4.2	None
213025700	Main Board for LT364 without HMM436's	6.4.2	None
213025678	Front Cover(4CH)for LT344/224	None	None
213025679	Front Cover(2CH) for LT342/322	None	None
213025680	8.4"Color TFT LCD Display Assy	None	None
213025615	Power Board	6.4.3	None
DMB020691	Floppy Disc Drive	None	None
213025681	Printer Assy	None	

The other parts are not on the above list because the probability of failure is very low. See chapter 7 and 8 for mechanical and electrical replaceable parts.

6.4 Board Exchange Procedure

6.4.1 Processor Board Exchange Procedure

The serial number of the LT Series oscilloscope is loaded in the real time clock memory which is battery backed up. If it becomes necessary to replace the processor board, the serial number must be loaded in the memory of the new board by using LeCroy program " LeCalsoft " under GPIB remote control.
To run " LeCalsoft " type SKP.exe, in the main menu type S, and follow the instructions, use five digits to enter the serial number (i.e. 10281).
Then check in the system summary, by using the show status button on the front panel, the scope serial number.

6.4.2 Main Board Exchange Procedure

After Main Board is exchanged, adjust as the following method.

- Assemble the lower cover and upper cover.
- Plug in the power cord and turn on the LT Series.
- Wait for fifteen minutes.
- Enter the internal menus by pressing menu soft-keys 3 & 4, then release soft-key 3, then release soft-key 4, then press soft-key 5.
- Select "**Maintenance**", "**Board Test Results**", "**Adjust**".
- Press "Measure **Board Items**", and wait till "Succeeded" is displayed.
- Press "Measure **Overload**", and wait till "Measure Complete" is displayed.
- Press "Save **Result to EEPROM**" two times.

Note ; Do not press the other menu keys, or some calibration data of Main Board may be lost.

This section does not include the other manual adjustments of Main Board, and does not contain any instructions or descriptions about Main Board calibration. Main Board adjustments required complex test set-up and calibration Software. For information on the availability of the tester and software, contact your nearest LeCroy service centre.

6.4.3 Power Board Exchange Procedure

After Power Board is exchanged, confirm the voltage as the following procedure.

- Remove the upper cover and the lower cover. (see 7.G)
- Turn the scope upside down.
- Turn on the power, set the scope to **Auto Trigger** and **500MS/s.**
- Confirm the following voltage on solder side of Main Board within ten minutes.

+12V analog	(Min = +11.76V, Max = +12.24V)	21C11
+5V analog	(Min = +4.925, Max = +5.075V)	21C21
-5V analog	(Min = -4.975V, Max = -5.05V)	21C71
-12V analog	(Min = -11.76V, Max = -12.24V)	21C61
+5V digital	(Min = +4.85V, Max = +5.15V)	21C41
-4.5V digital	(Min = -4.365V, Max = -4.635V)	21C91

Note ; Do not turn the potentiometers on Power Board.
Do not keep the condition that the lower cover is removed, or the heat sinks will become hot and the condition may damage some components on Main Board.

This section does not include the other manual adjustments of Power Board, and does not contain any instructions or descriptions about Power Board calibration. Power Board adjustments required complex test set-up.
For information on the availability of the tester, contact your nearest LeCroy service centre.

6.5 Troubleshooting and Flow Charts

6.5.1 Introduction

The troubleshooting information contained in this section is intended for use by qualified personnel having a basic understanding of electronics (analog and digital). In order to simplify servicing and minimise downtime, the following list of possible symptoms, likely causes, and troubleshooting steps have been prepared.
The first step in troubleshooting is to check for obvious items like blown fuses.
The power supply is the next item to check before proceeding to more detailed troubleshooting, since noise or low power supply voltages can cause a variety of digital and analog problems.

6.5.2 Line Fuses Replacement

The power supply of the oscilloscope is protected against short circuits and overload by means of two T6.3A / 250 V fuses located above the main plugs.

Turn off the power and disconnect the line cord from the instrument Disconnect the instrument from other equipment.

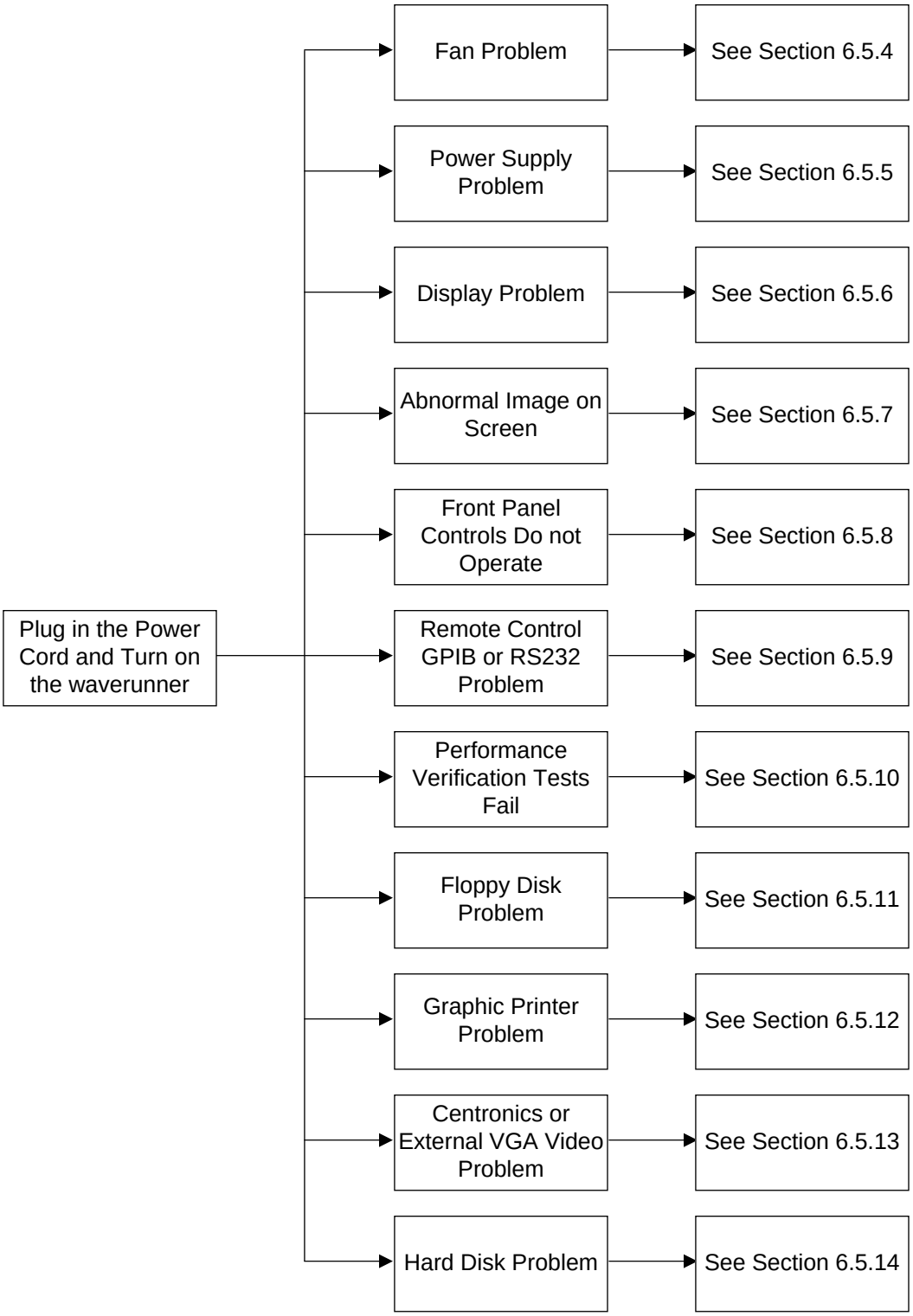
To replace line fuses, proceed as follow:

- Open the fuse box by inserting a small flat screwdriver under the plastic cover and remove the fuse carrier from the holder
- Remove the fuse and replace it with the proper type: T6.3 A / 250 V, LeCroy part number: **433 162 630**

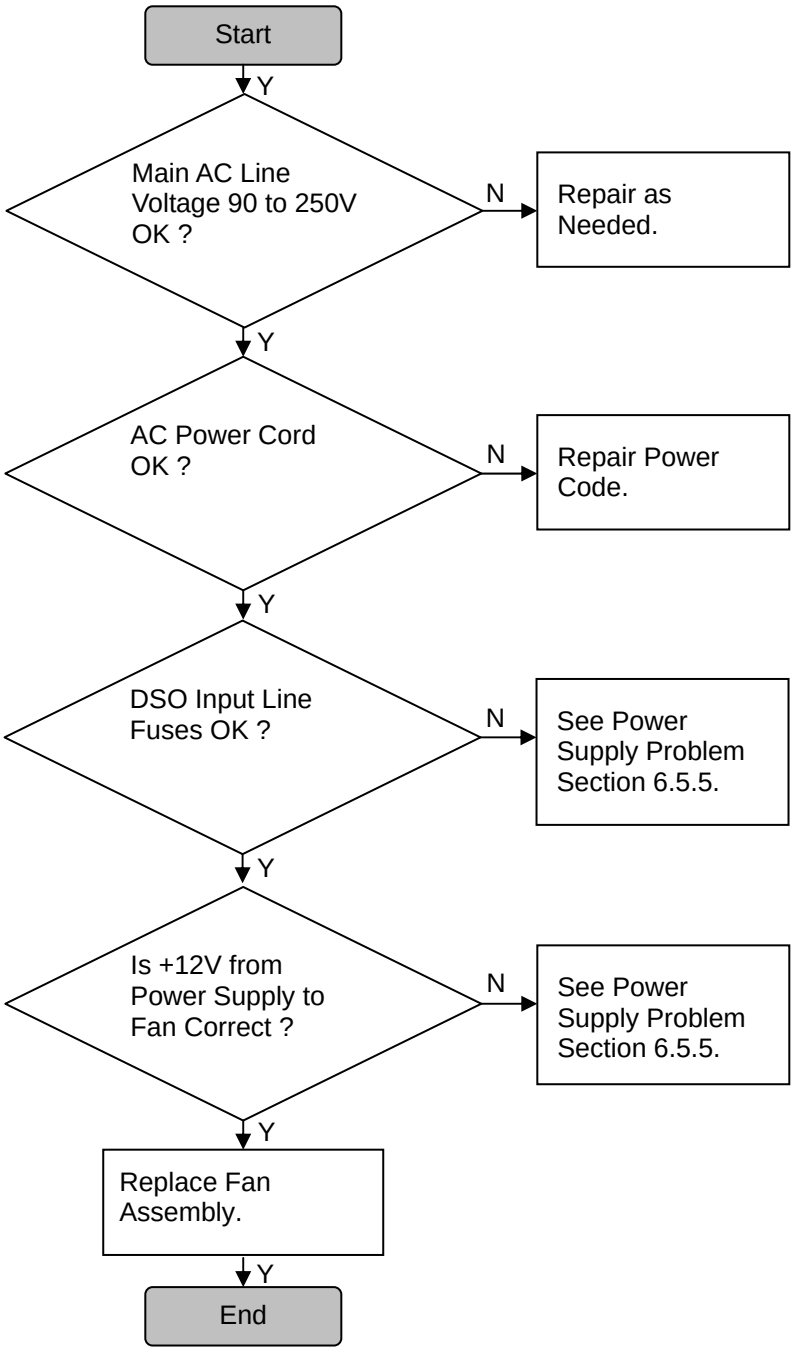
6.5.3 Initial Troubleshooting Chart

Most procedures in this section will allow troubleshooting down to the **BOARD LEVEL.**

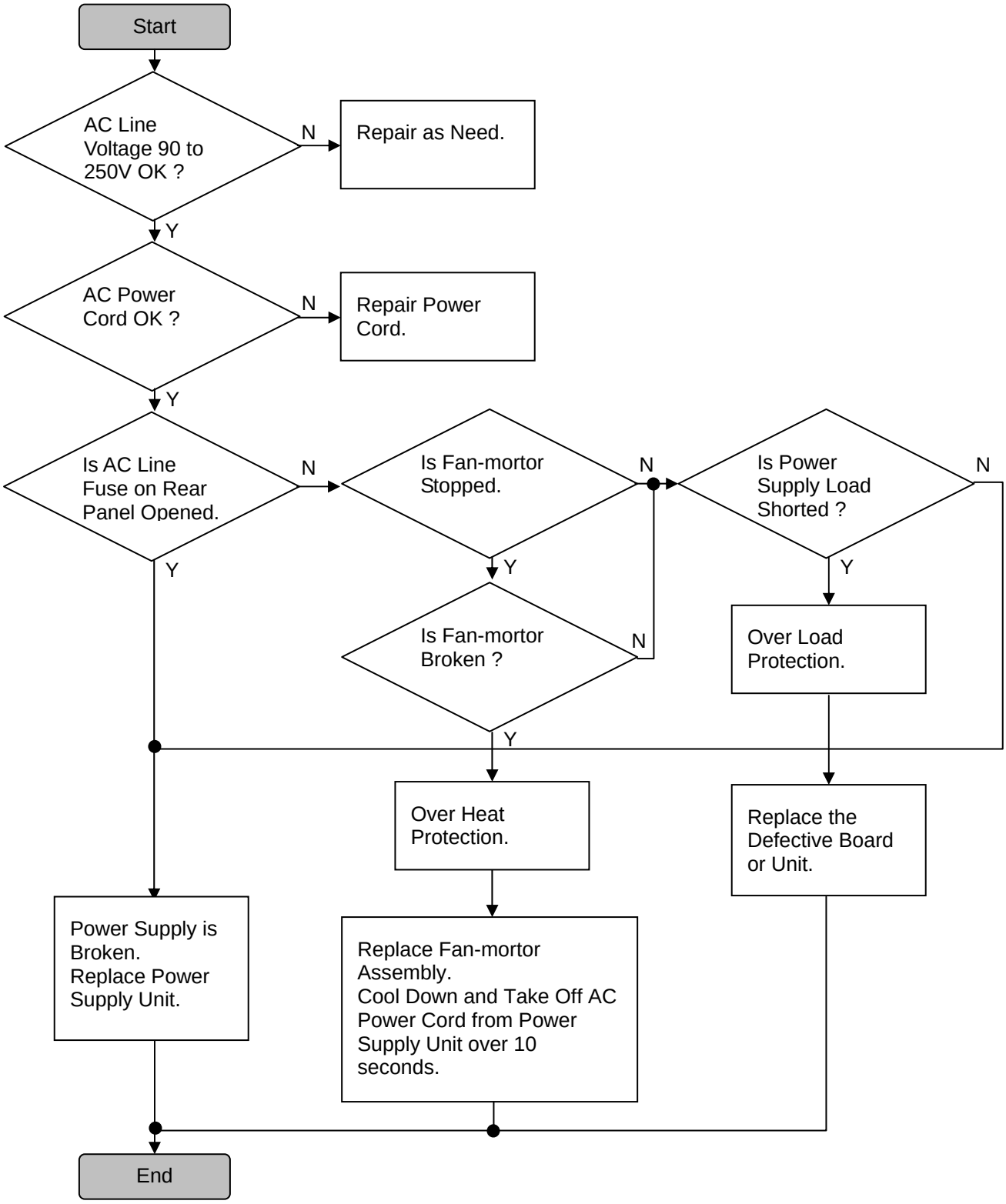
Defective circuit boards will be repaired or exchanged by the regional LeCroy service office or the local representative (see section 2.2).


Plug in the Power Cord and Turn on the waverunner
Fan Problem
See Section 6.5.4
Power Supply Problem
See Section 6.5.5
Display Problem
See Section 6.5.6
Abnormal Image on Screen
See Section 6.5.7
Front Panel Controls Do not Operate
See Section 6.5.8
Remote Control GPIB or RS232 Problem
See Section 6.5.9
Performance Verification Tests Fail
See Section 6.5.10
Floppy Disk Problem
See Section 6.5.11
Graphic Printer Problem
See Section 6.5.12
Centronics or External VGA Video Problem
See Section 6.5.13
Hard Disk Problem
See Section 6.5.14

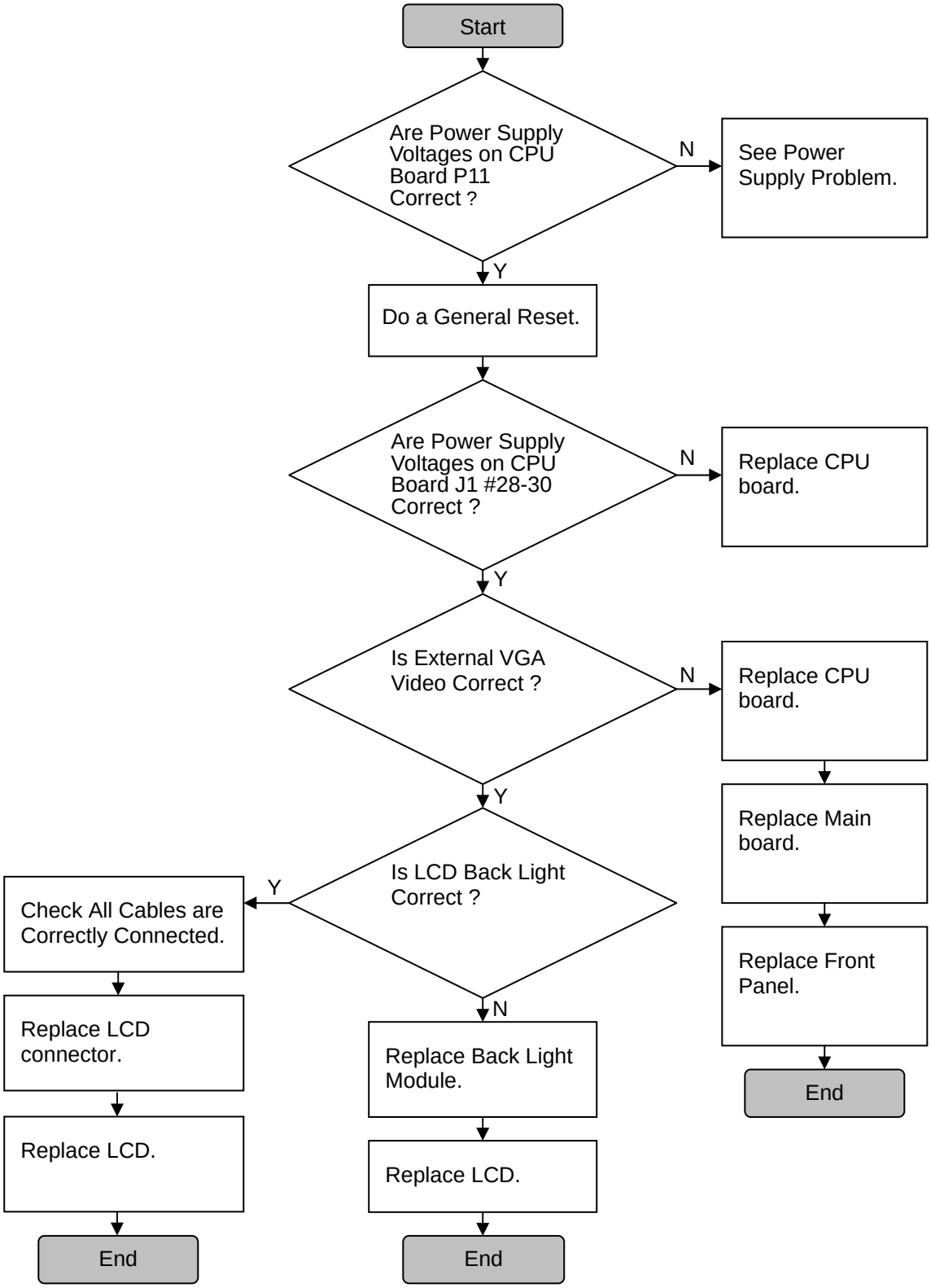
6.5.4 Fan Problem



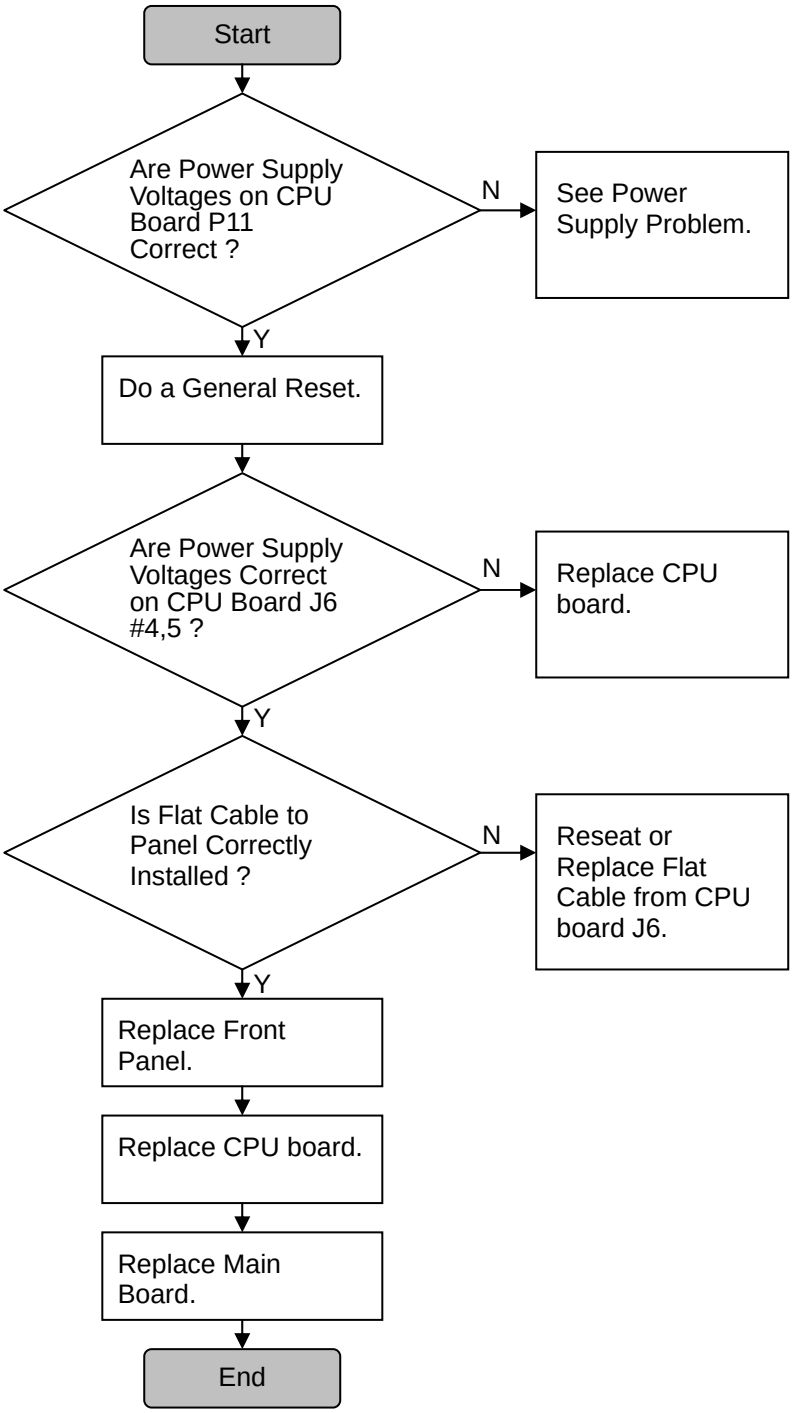
6.5.5 Power Supply Voltage Problem



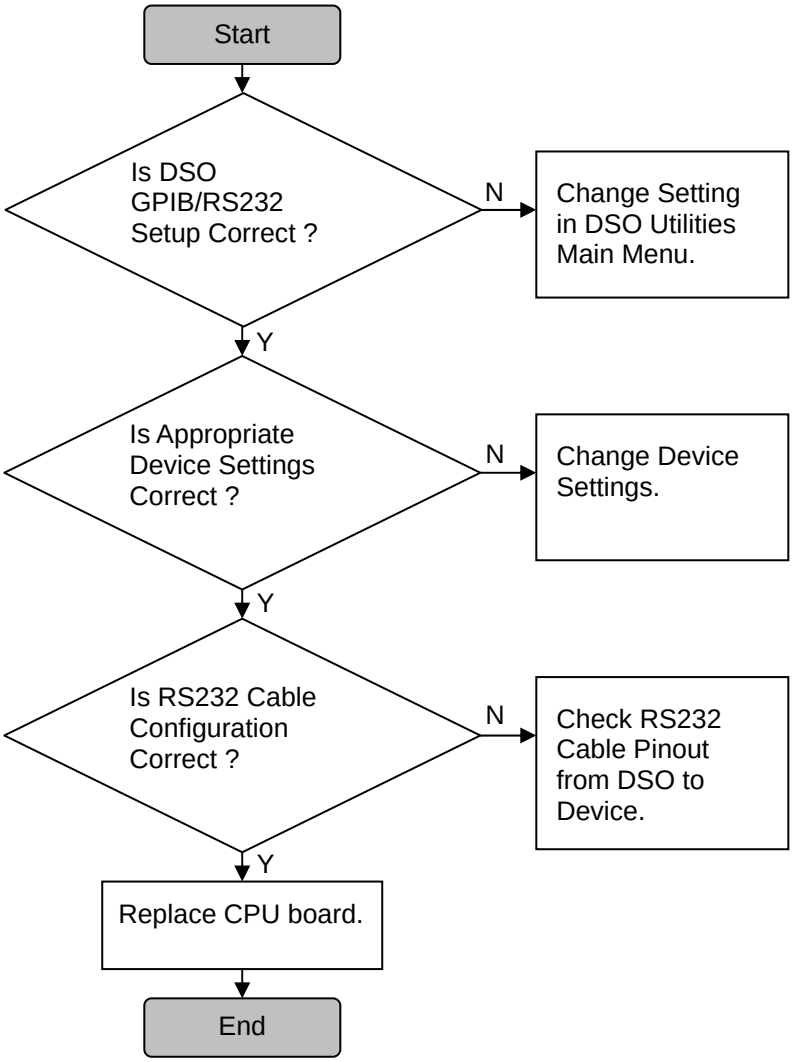
6.5.6 Display Problem



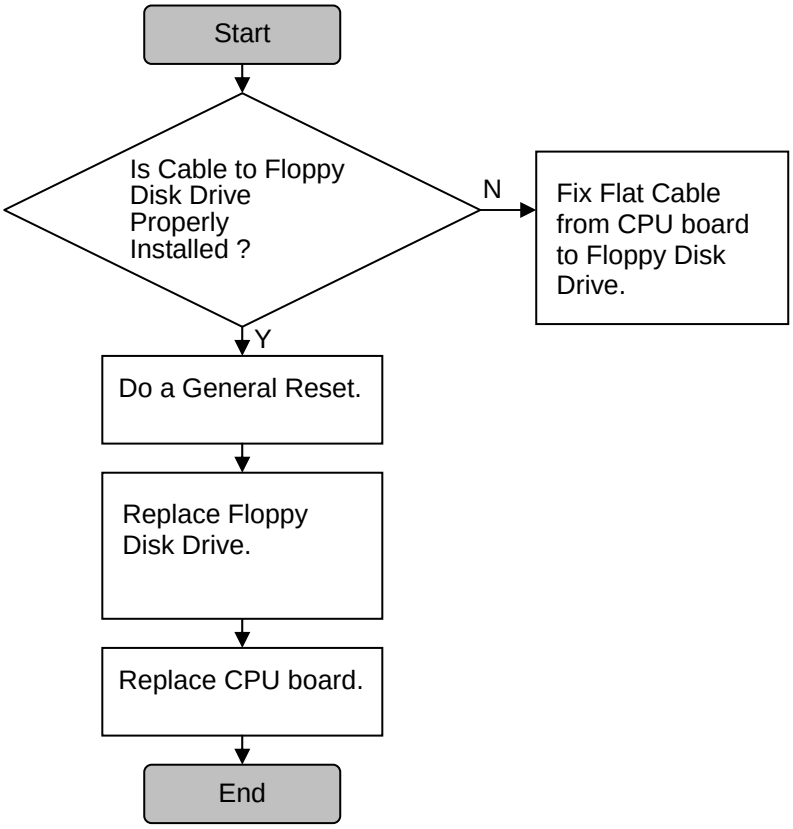
6.5.7 Front Panel Controls Do not Operate



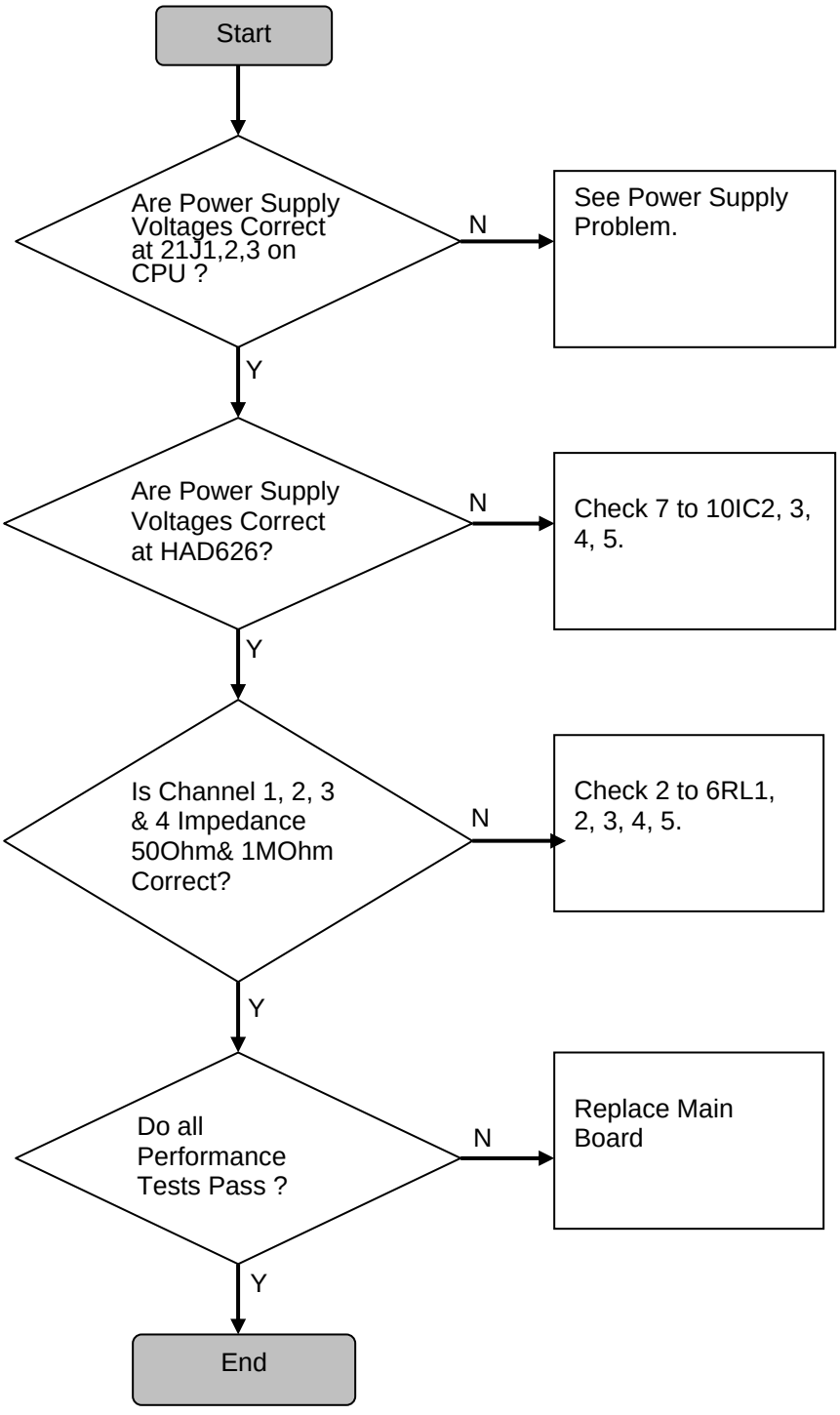
6.5.8 Remote Control GPIB or RS232 Problem



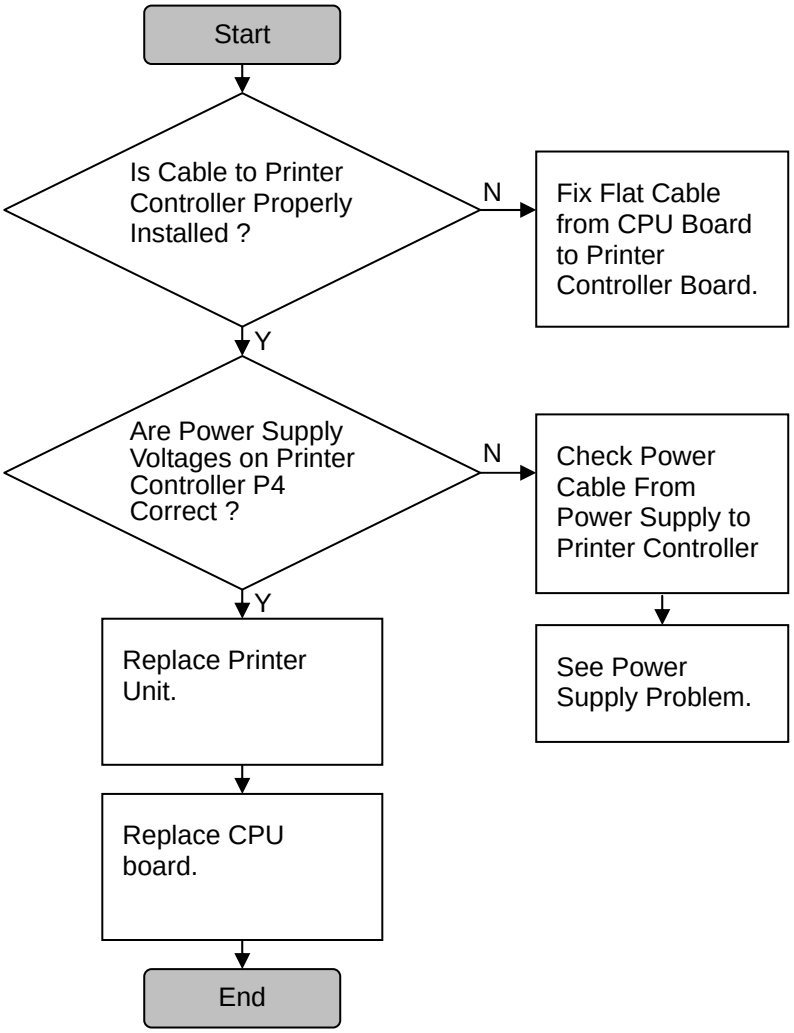
6.5.9 Floppy Disk Drive Problem



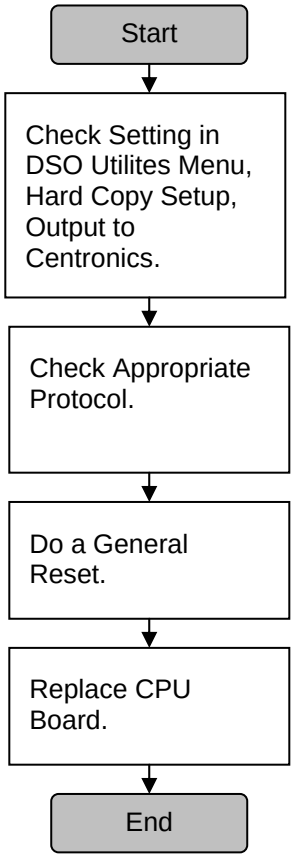
6.5.10 Performance Verification Fails



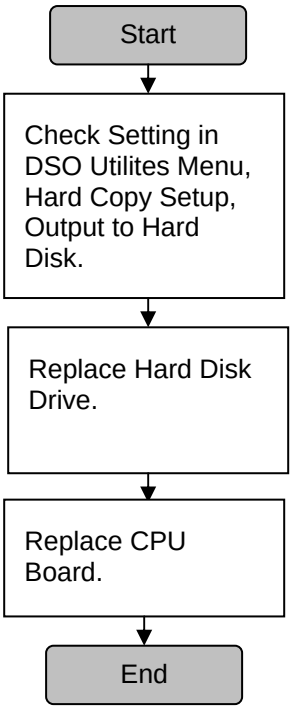
6.5.11 Graphic Printer Problem



6.5.12 Centronics Problem



6.5.13 Hard Disk Drive Problem

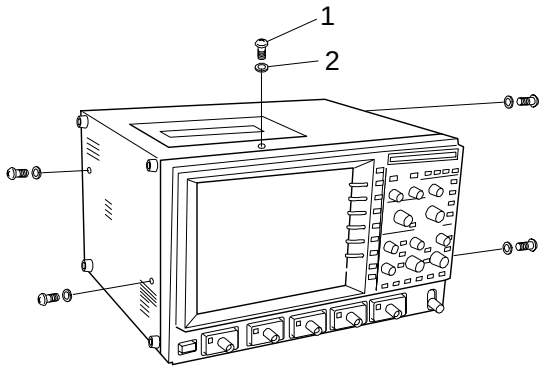


7. Mechanical Parts & Removal

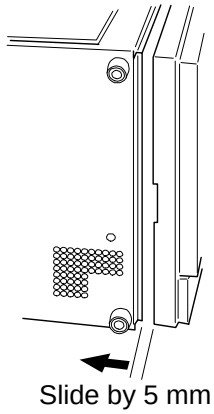
A. Removal of the Upper Cover Assembly (with printer)

- A1, A2 : Remove the nine M3 x 6 screws with nylon washer (one on the top/each two on the right and left sides/four on the rear).
- A3 : In the case of a unit with a built-in printer (option), open the printer cover and depress the locking latch.
- A4 : Slide the upper cover rearward by approx. 5 mm. It is firm.
- A5 : Remove the upper cover by opening and lifting the lower portion of the cover.

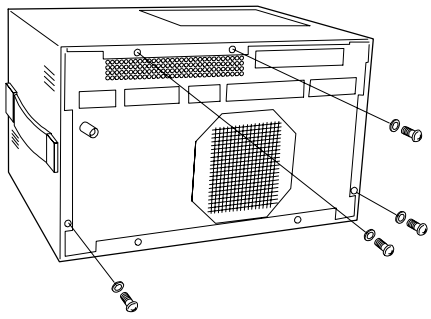
[A1]



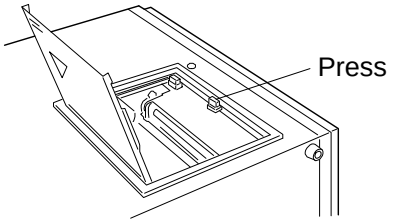
[A4]



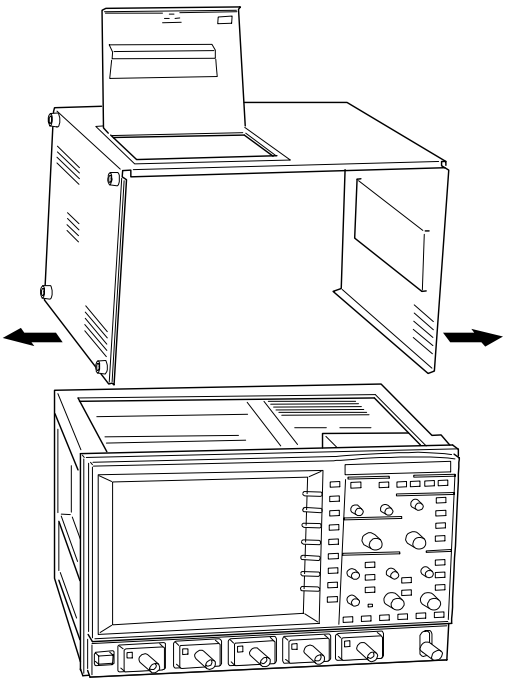
[A2]



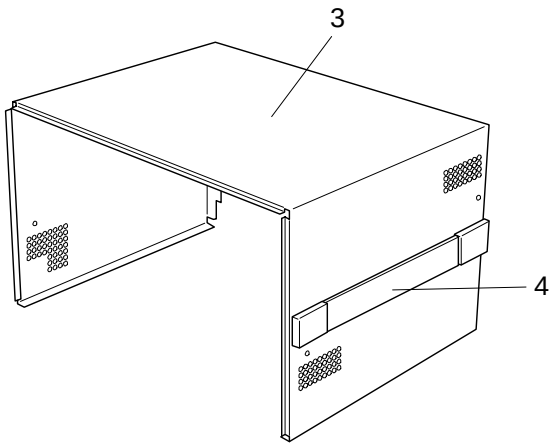
[A3]



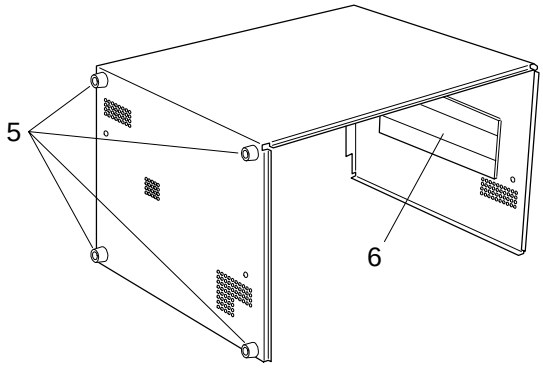
[A5]



[A6]



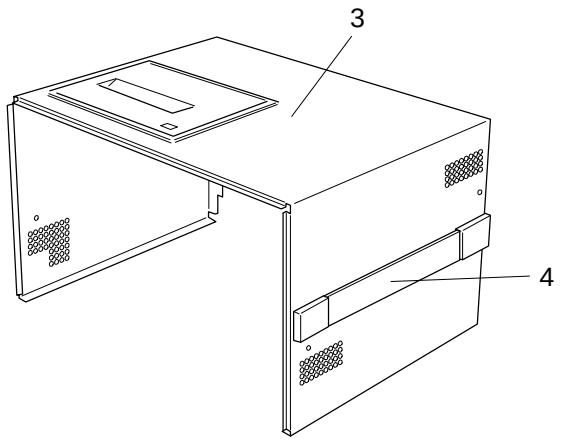
[A7]



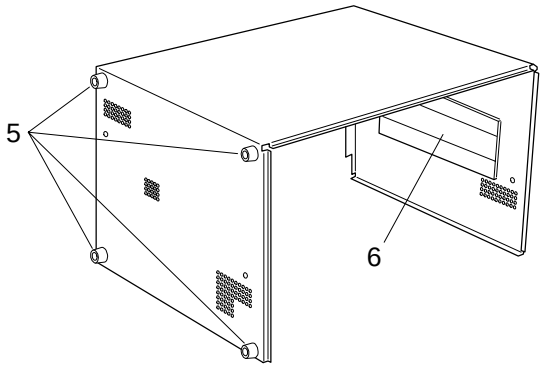
Upper Cover Replaceable Parts

Item	IWATSU Part Number	Quantity	Description
1	MKB130062	9.0	Screw M3x6
2	MPW930000	9.0	Washer W-3, nylon
3	KBA787311	1.0	STD TOP COVER LE
4	MTH000791	1.0	Handle THA-238-L260 UL-I
5	MGA000721	4.0	Side Foot 5475 UL-I
6	KPL142611	3.0	Cushion
3, 4, 5, 6	21302-5676	1.0	LT UPPER COVER ASSY

[A8]



[A9]

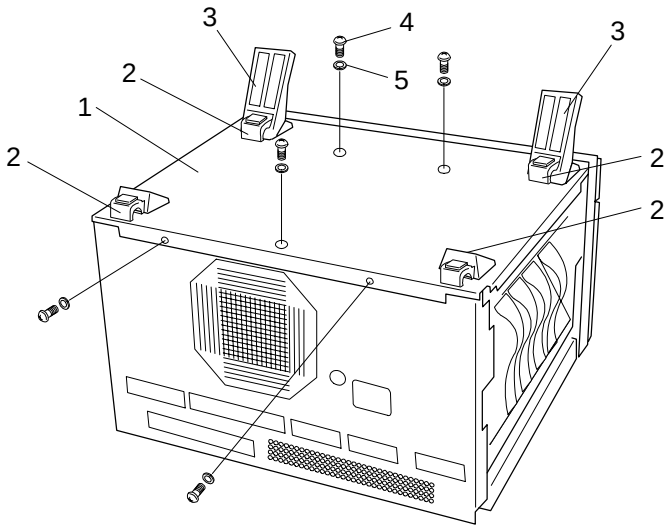


Upper Cover (with a built-inprinter) Replaceable Parts

Item	IWATSU Part Number	Quantity	Description
1	MKB130062	5.0	Screw M3x6
2	MPW930000	5.0	Washer W-3, nylon
3	KBA786321	1.0	TOP COVERL E
4	MTH000791	1.0	Handle THA-238-L260 UL-I
5	MGA000721	4.0	Side Foot 5475 UL-I
6	KPL142611	3.0	Cushion
7	KCM141411	1.0	PRINTER COVER FRAME UL-I
8	KCM141311	1.0	PRINTER COVER UL-I
3, 4, 5, 6, 7, 8	21302-5677	1.0	LT UPPER COVER(GP02) ASSY

B. Removal of the Bottom Cover Assembly

- Remove the upper cover.
- Remove the five M3 x 6 screws (with nylon washer, 3 on the bottom/2 on the rear).



Bottom Cover Replaceable Parts

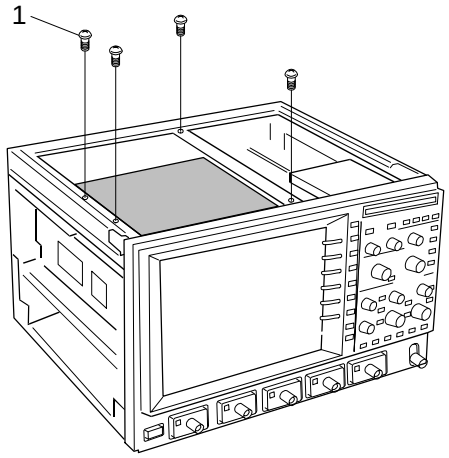
Item	IWATSU Part Number	Quantity	Description
1	KBA786921	1.0	BOTTOM COVER LE
2	KAS137811	4.0	BOTTOM FOOT ASSY
3	KCM131421	2.0	Rotor for the tilt stand
4	MKB130062	5.0	Screw M3x6
5	MPW930000	5.0	Washer W-3, nylon

C. Removal of the Printer Assembly

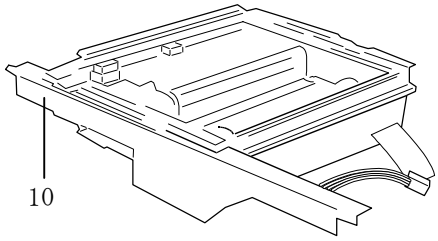
Remove the upper cover.

- C1 : Remove the four M3 x 6 screws (2 on the TOP FRAME L/2 on the center frame).
- C2 : Remove the CPU J7/FFC cable.
- C2 : Remove the POWER BOARD CN6/power 3P cable.

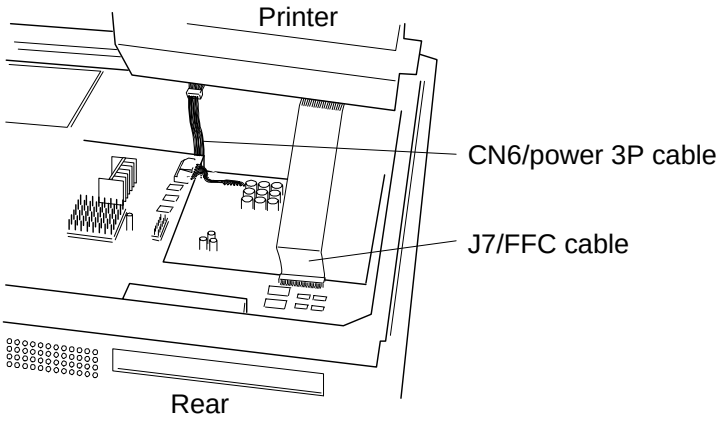
[C1]



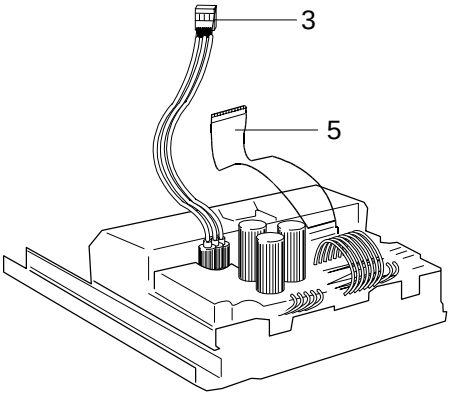
[C3]



[C2] View as the rear side of the printer unit lifted



[C4]



Printer Parts

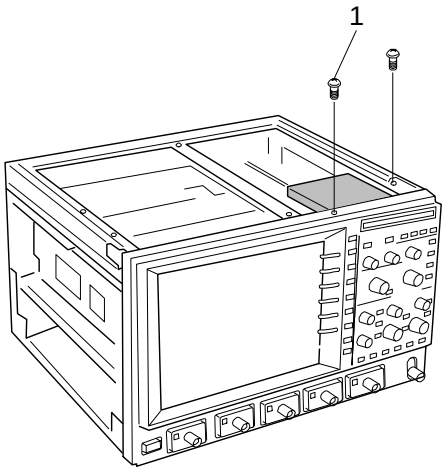
Item	IWATSU Part Number	Quantity	Description
1	MKB130062	4.0	Screw KB(+)3X6S(NIP)
2	DZB992361	1.0	PRINTER FTP-642MCL001
3	KHB189311	1.0	PRINTER POWER CABLE UL-I
4	KHB189611	1.0	PRINTER HEAD CABLE UL-I
5	AHB202811	1.0	FFC-26P-L140-P1/CPU
6	KCM141211	1.0	PRINTER CASE UL-I
7	MFA001471	1.0	TL-304-1
8	KBA785511	1.0	PRINTER BASE UNIT
9	MSQ901661	3.0	Screw TT2(+)3X8S
10	KBA786211	1.0	CENTER FRAME
11	MKB130062	2.0	Screw KB(+)3X6S(NIP)
12	MSQ903531	3.0	Screw S-tight KB(+)2.5X6S
13	MKB130062	4.0	Screw KB(+)3X6S(NIP)
14	MHK000961	1.0	BAND CV-70/YJ-80
15	KCM142121	1.0	TKM KEYTOP B- GR UL-I
2 to 15	21302-5681	1.0	LT PRINTER UNIT(GP02) See Fig [C3, C4]

D. Removal of the Floppy Assembly

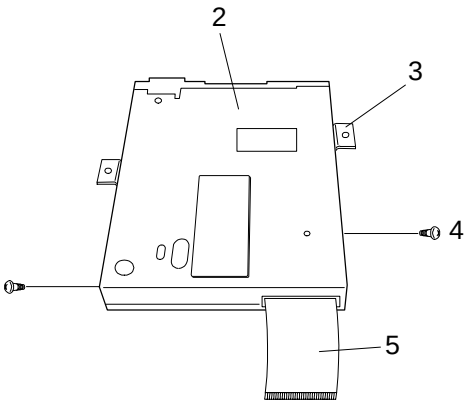
Remove the upper and bottom covers.

- D1 : Remove the CPU BOARD J2/FFC cable from the CPU.
- D1 : Remove two M3 x 6 screws on the TOP FRAME R and FRONT FRAME A.

[D1]



[D2]



Floppy Replaceable Parts

Item	IWATSU Part Number	Quantity	Description
1	MKB130062	2.0	Screw M3x6
2	DMB020691	1.0	FD DRIVE WIDE-00B See Fig [D2]
3	KBA785211	1.0	FDD SUPPORT PLATE
4	MSQ903521	2.0	Screw M2.5x4

E. Removal of the CPU Board

Remove the upper and bottom covers.

Remove the printer and floppy.

Remove the four M3 x 6 screws from the right and left frame.

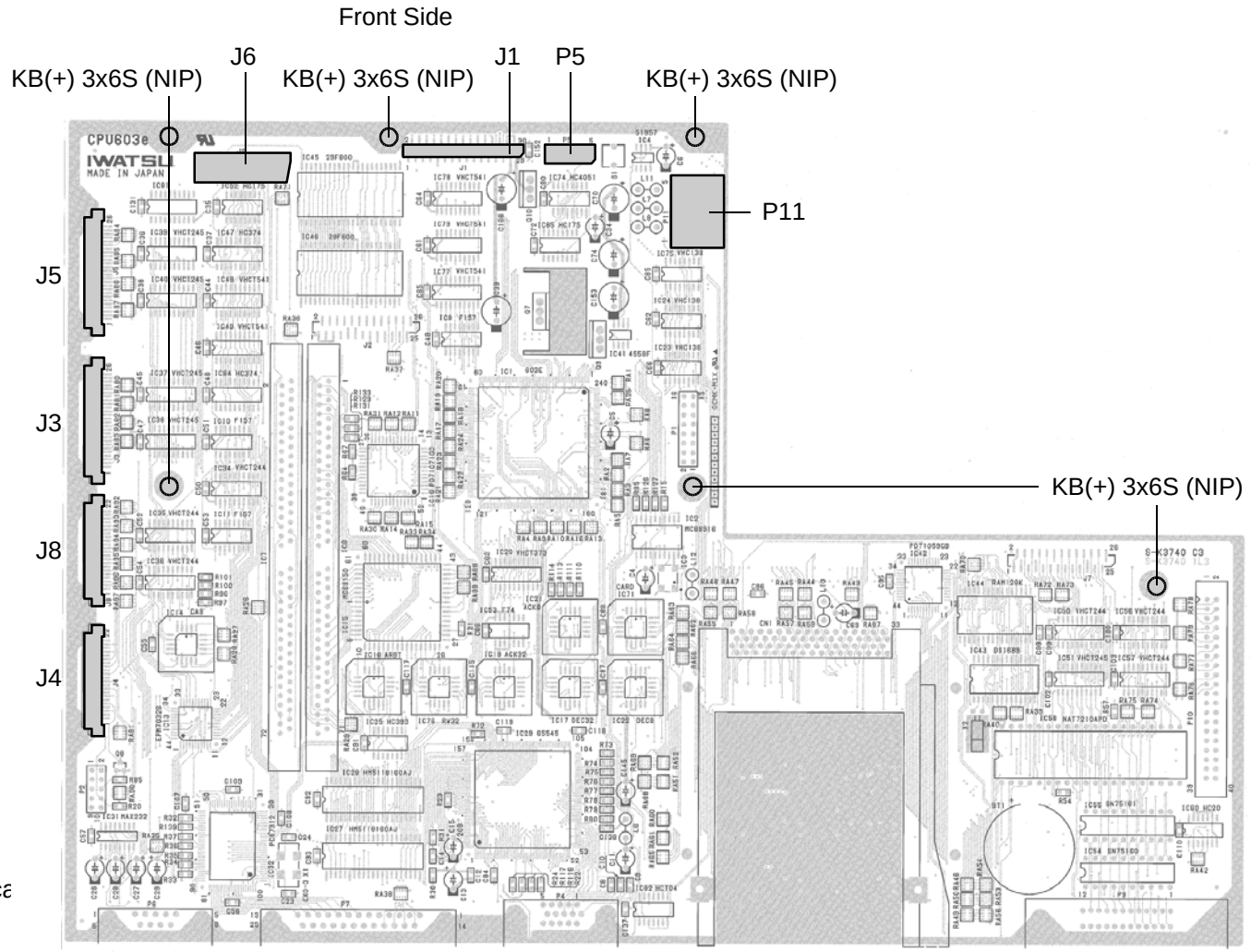
[Note] Remove the cables on the CPU Board and next the screws on it.

- E1 : Remove the four FFC cables on the CPU Board (J3/26pin, J4/22pin, J5/26pin, J8/22pin).
- E1 : Remove the two FFC cables on the CPU Board (J1/30pin, J6/22pin).
- E1 : Remove the P5 power connector on the CPU Board (to LCD).
- E1 : Remove the P11 power connector on the CPU Board (to POWER).
- E2 : Remove the four M3 x 6 screws (4 on the rear, fastening between connectors and between the rear panel and CPU).

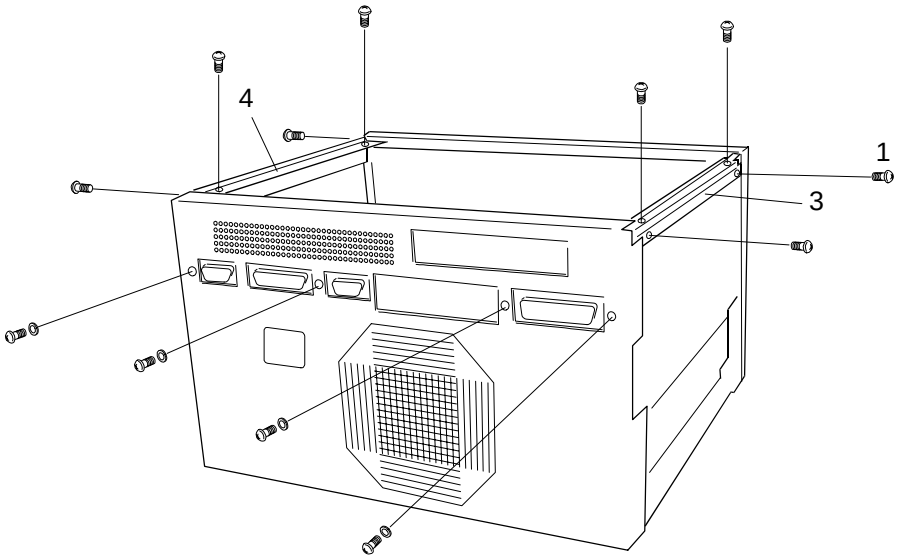
  Remove the eight M3x6 screws on the TOP FRAME L and R.
- E3 : Remove the six M3 x 6 screws on the CPU Board and remove the processor broad by sliding it toward the front side.

Caution : Batteries are mounted, so care should be taken to prevent short-circuiting.

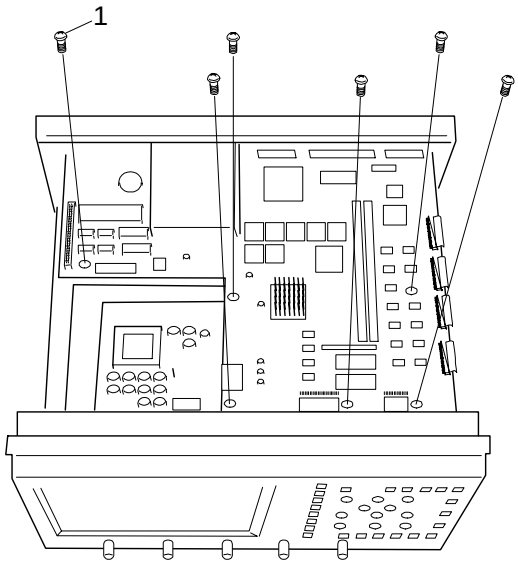
[E1]



[E2]



[E3]



CPU Board Replaceable Parts

Item	IWATSU Part Number	Quantity	Description
1	MKB130062	18.0	Screw M3x6
2	21302-5610	1.0	CPU BOARD ASSY
3	KBA784421	1.0	TOP FRAME L
4	KBA784511	1.0	TOP FRAME R

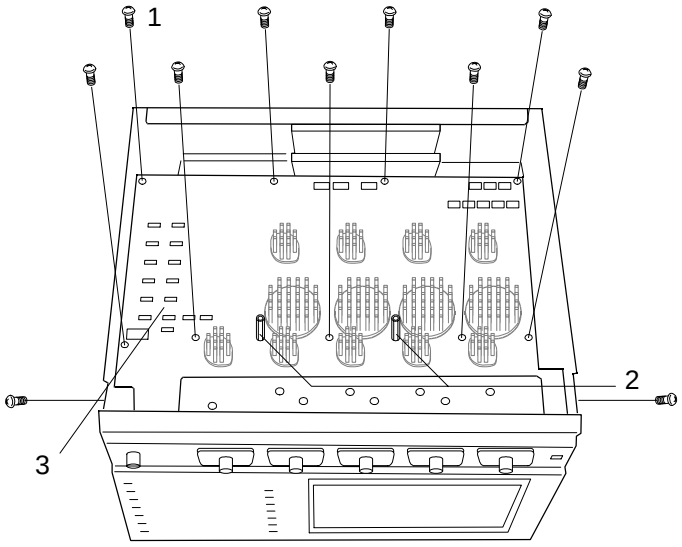
F. Removal of the Main Board

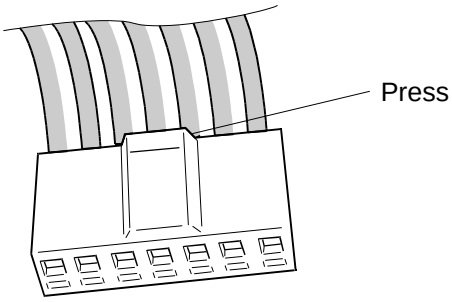
Remove the upper and bottom covers.

[Note] Remove the cables on the Main Board and next the screws on it.

- F1 a/b : Remove the four FFC cables (20J1/26pin, 20J4/22pin, 20J2/26pin, 20J3/22pin).).
- F1 a/b : Remove the Signal out connector (16J2).
- F1 a/b : Remove the 7P power connectors (21J1, 21J2, 21J3) while pressing the stopper of 21J1 and 21J2.
- F1 a/b : Remove the two support PNC20 from the main board.
- F1 a/b : Remove the nine M3 x 6 screws (on the Main Board).
- Remove the main board by lifting its rear side slightly and sliding it rearward.

[F1a]



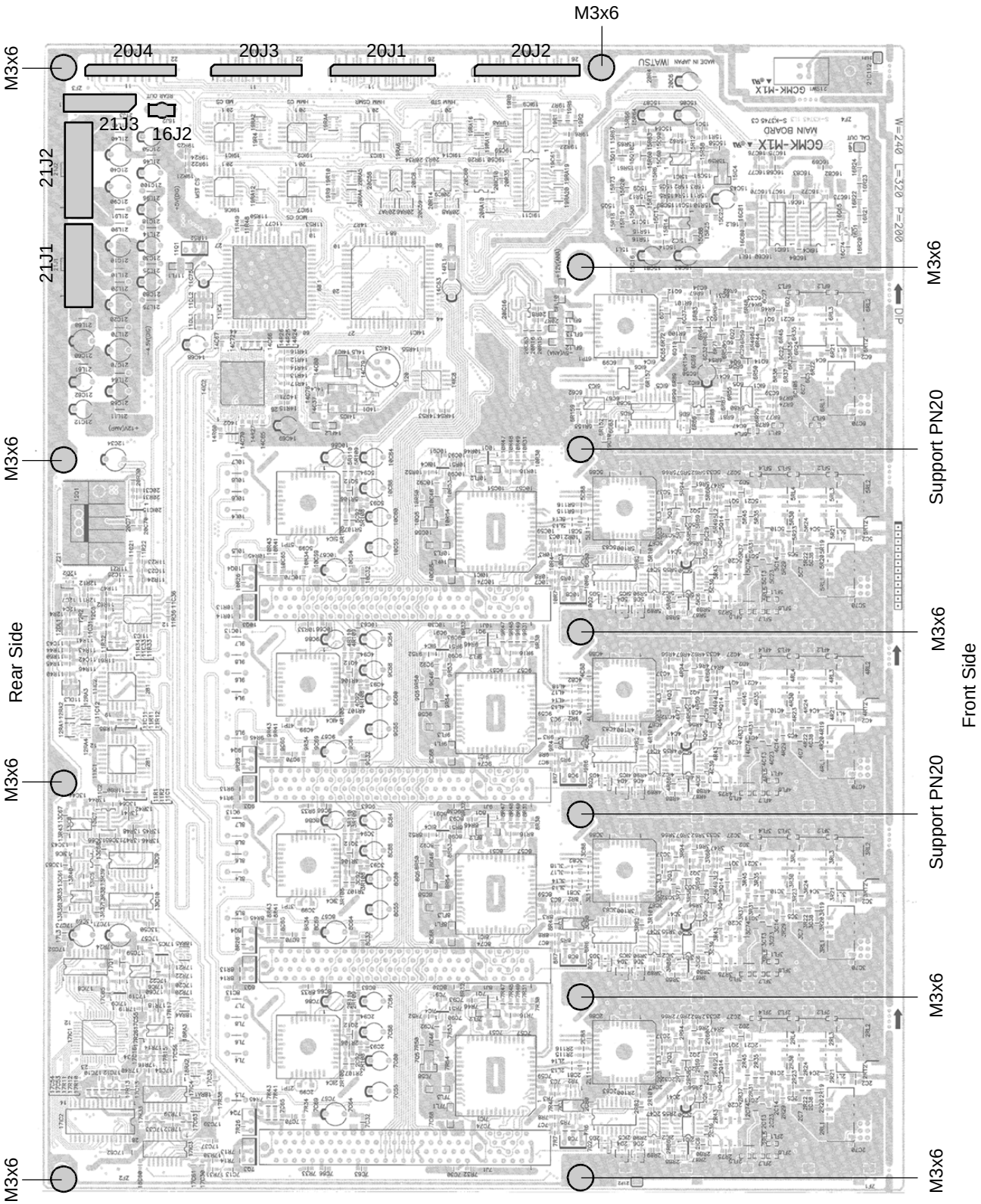


21J1, 21J2

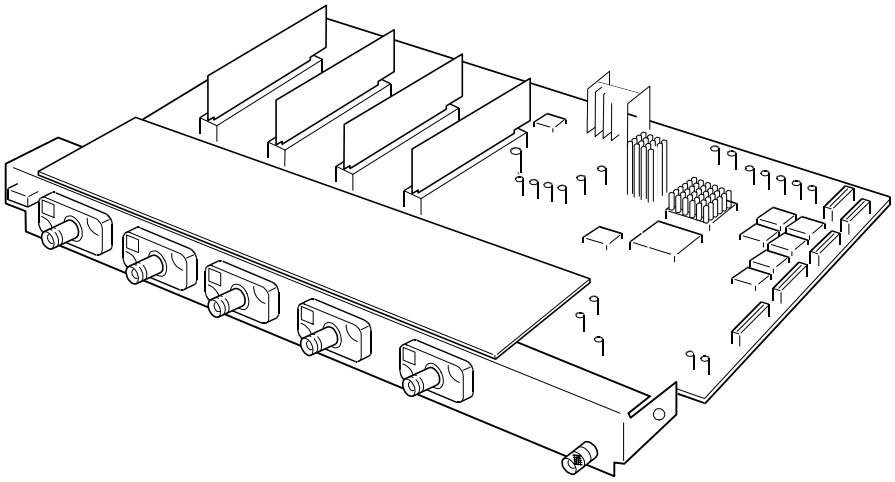
Main Board Replaceable Parts

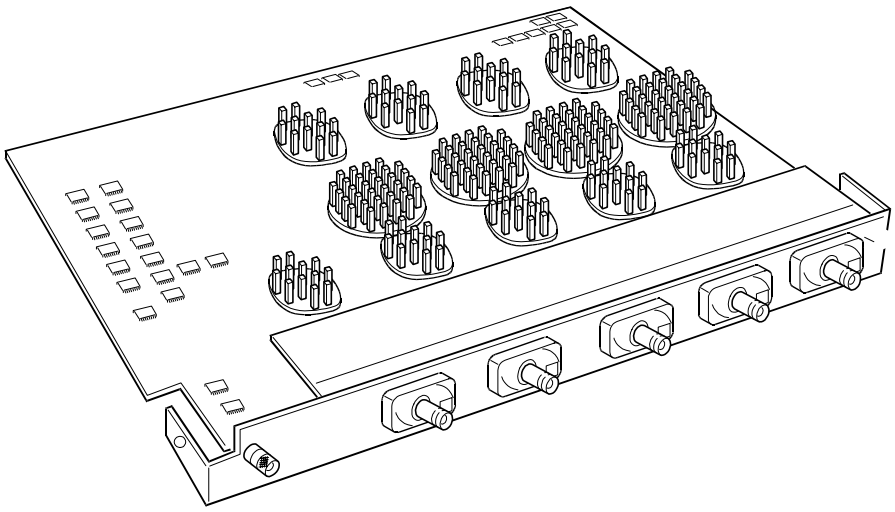
Item	Part Number	Quantity	Description
1	MKB130062	11.0	Screw M3x6
2	MZT902191	2.0	Metallic support PNC20
3	213025605 213025650 213025648 213025670 213025700	1.0 1.0 1.0 1.0 1.0	MAIN BOARD ASSYSee Fig [F2] LT344/344L LT342/342L LT322 LT224 LT364/364L

[F1b]


M3x6
20J4
20J3
20J1
20J2
21J3
16J2
21J2
21J1
M3x6
M3x6
Support PN20
M3x6
Rear Side
Front Side
M3x6
Support PN20
M3x6
M3x6
M3x6

[F2]





G. Removal of the Power Supply Assembly

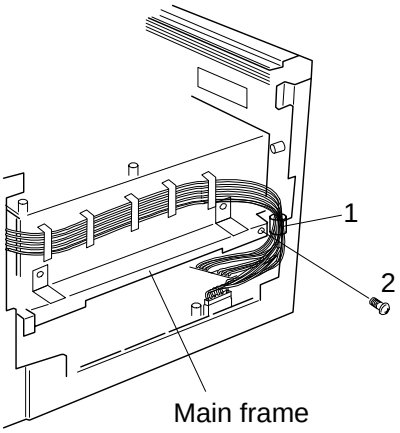
Remove the upper and bottom covers.

Remove the processor assembly.

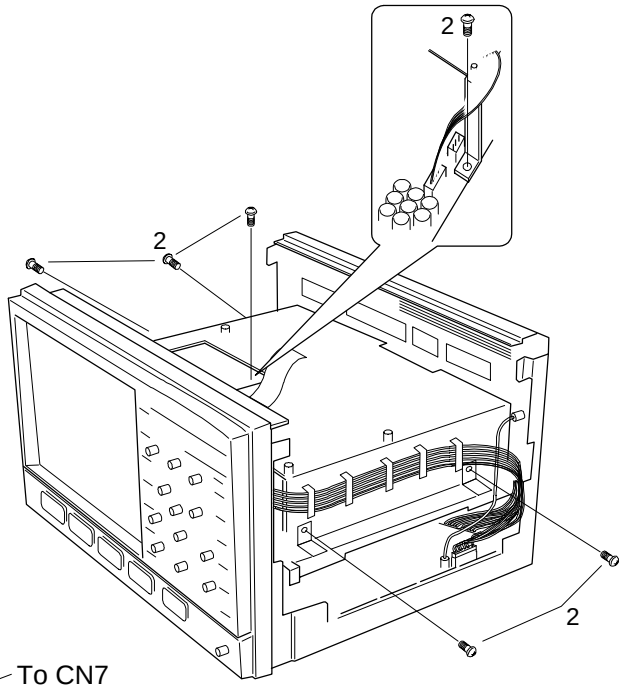
Remove the main assembly.

- G1 : Remove the Harnessing belt on the main frame.
- G2 : Remove the connector (CN7) on the Power board from the fan.
- G2, G3 : Remove the seven M3 x 8 screws (2 on the rear inlet/4 on either side/1 on the top).

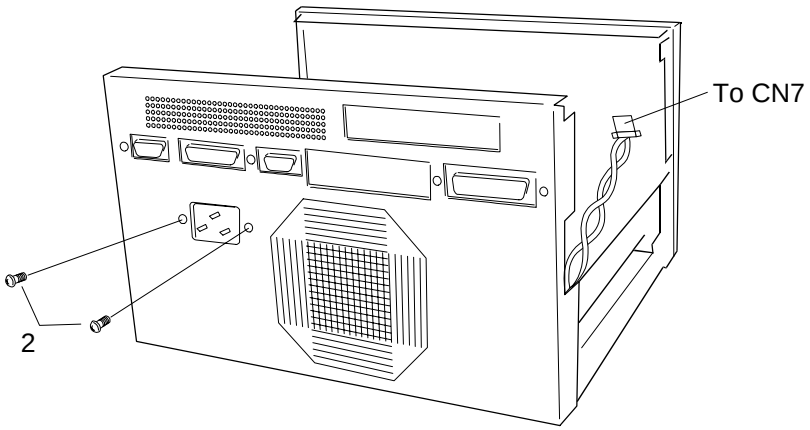
[G1]



[G3]



[G2]



Power Board Replaceable Parts

Item	IWATSU Part Number	Quantity	Description
1	MHK001541	1.0	Harnessing belt SL-9N
2	MKB130082	8.0	Screw M3x8
3	21302-5615	1.0	Power Board ASSY

H. Removal of the Front Panel Assembly

Remove the upper and bottom covers.

Remove the processor assembly.

Remove the main assembly.

Remove the power supply assembly.

- H1 : Remove the two M3x6 screws that secure the front panel assembly and the main frame.
- H1 : Remove the three M3 x 6 screws on the each side frames R and L.
- H2 : Inverter plate: Remove the two M3 x 6 screws.
- H2 : Inverter board: Remove the two tap tight M2 x 6 screws.
- H2 : Remove the eight a screws that secure the BEZEL and FRONT FRAM A/B.

LCD Assembly : H3, H4, H5

- H3 : Remove the four LCD mounting screws.
- H4 : Remove the connection board between LCD and KEY BOARD while holding the connectors.

FRONT PANEL ASSY : Remove the knobs.

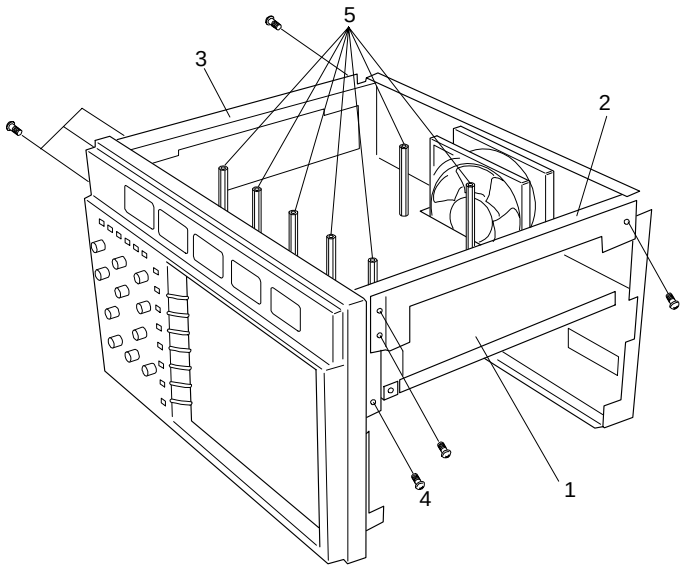
- H6 : Remove the nine screws that secure BEZEL and KEY BOARD.

  Caution : knob12 UL-1(4)TIME/DIV, VOLTS/DIV, ZOOMx2

  knob09 UL-1(7)

  How to insert knobs : Match the straight portions.

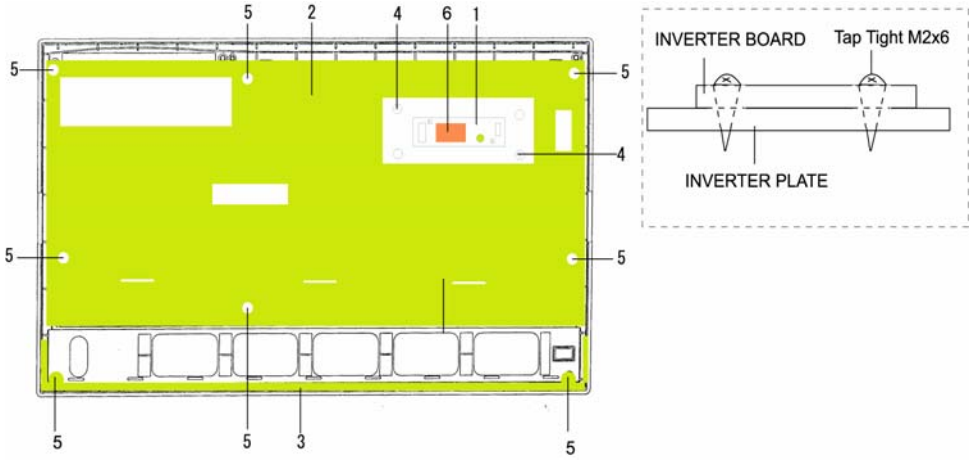
[H1]



H1 Replaceable Parts

Item	IWATSU Part Number	Quantity	Description
1	KBA784011	1.0	MAIN FRAME
2	KBA784911	1.0	SIDE FRAME L
3	KBA785011	1.0	SIDE FRAME R
4	MKD130061	4.0	Screw M3x6
5	MZT903161	7.0	Metallic support PSC60

[H2]

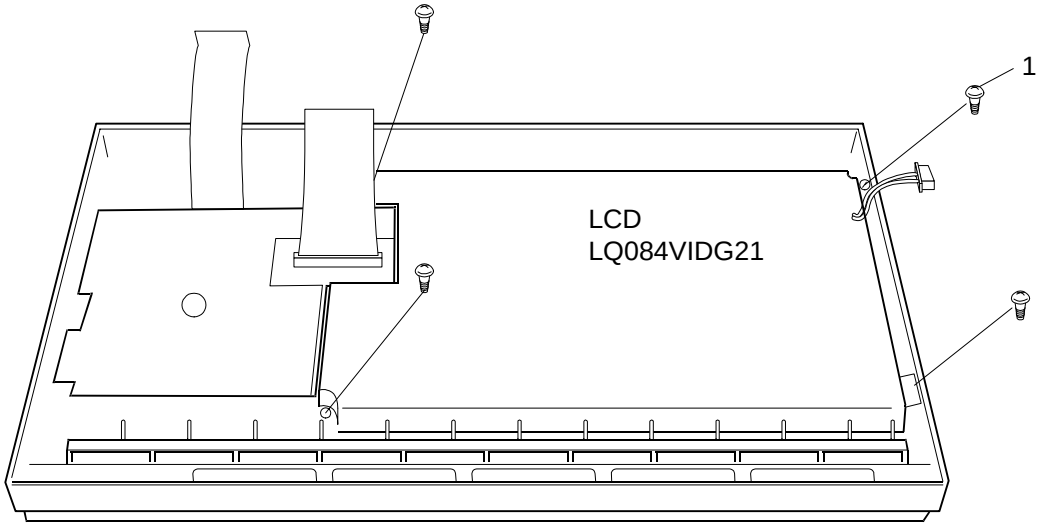


H2 Replaceable Parts

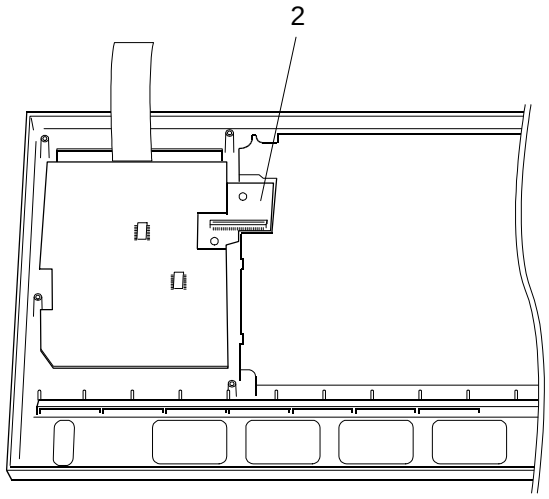
Item	IWATSU Part Number	Quantity	Description
1	KPL143211	1.0	INVERTER PLATE UL-1
2	KBA784121	1.0	FRONT FRAME A
3	KBA784211	1.0	FRONT FRAME B
4	MKB130062	2.0	Screw M3x6
5	MSQ901661	8.0	Screw TT2(+) 3x8S
6	DES040271	1.0	DC-AC INVERTER S-12598-5M

LCD Assembly

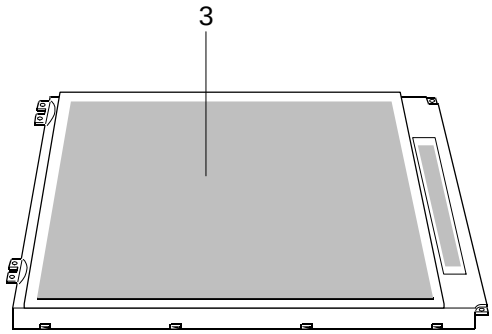
[H3]



[H4]



[H5]

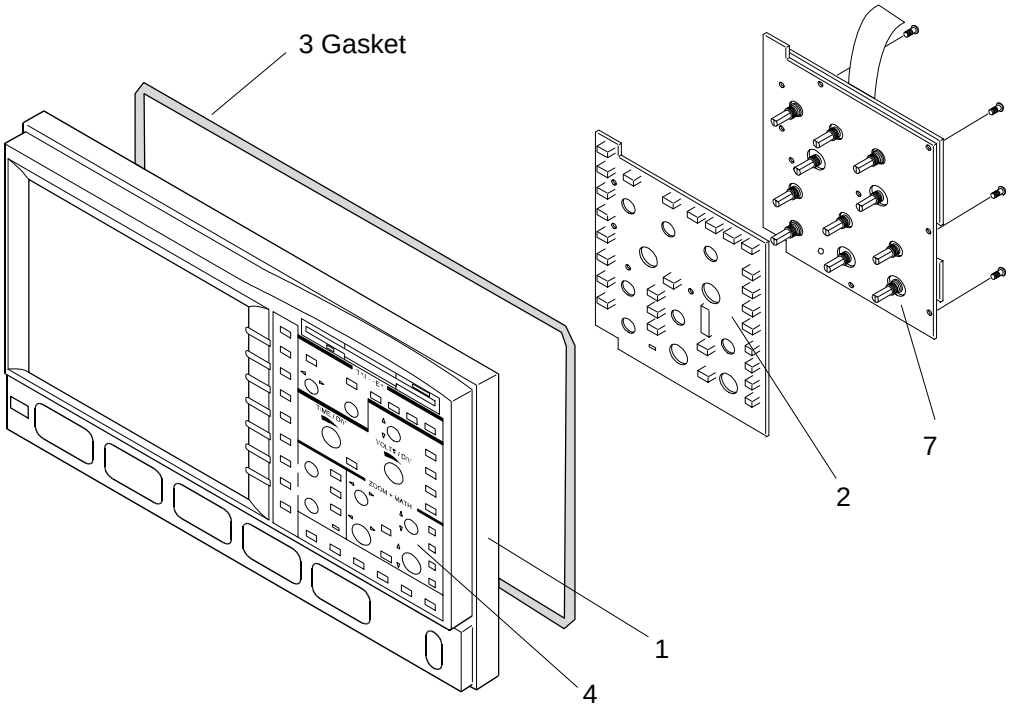


H3 to H5 Replaceable Parts

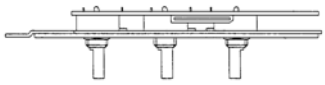
Item	IWATSU Part Number	Quantity	Description
1	MSQ903511	4.0	Screw PKB 2.5x8S
2	21302-5615	1.0	LCD CONNECTOR BOARD UL-M
3	21302-5680	1.0	LT LCD UNIT See Fig [H5]

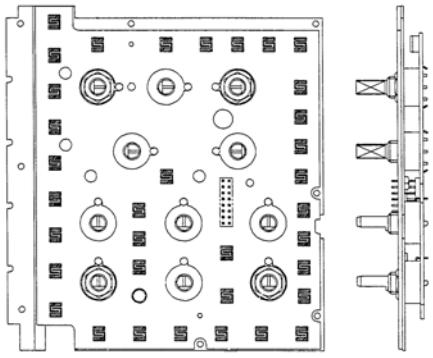
FRONT PANEL ASSY

[H6]

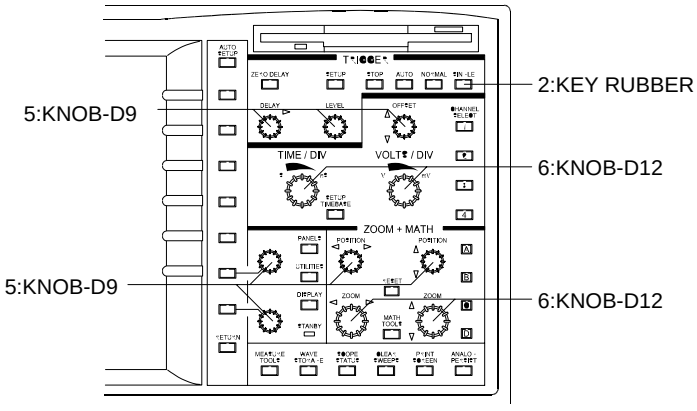


[H7]





[H8]



LT344/224 FRONT PANEL ASSY

Item	IWATSU Part Number	Quantity	Description
1	KCM140911	1.0	BEZEL FND14 UL-1
2	KGM029711	1.0	FND14 KEY PUBBER UL-I
3	MZT007871	1.0	GASKET UC-3E0564 UL-I
4	KPA219011	1.0	LT344 CONTROL PANEL UL-I
5	KCM141021	7.0	KNOBE-D9 UL-I
6	KCM141121	4.0	KNOBE-D12 UL-I
7	21302-5613	1.0	PANEL & KEY BOARD See Fig [H7]
1 to 7	21302-5678	1.0	LTxx4 FRONT PANEL(4CH) See Fig [H6]

LT342/322 FRONT PANEL ASSY

Item	IWATSU Part Number	Quantity	Description
1	KCM143211	1.0	BEZEL FND12 UL-1
2	KGM029711	1.0	FND14 KEY PUBBER UL-I
3	MZT007871	1.0	GASKET UC-3E0564 UL-I
4	KPA219111	1.0	LT342 CONTROL PANEL UL-I
5	KCM141021	7.0	KNOBE-D9 UL-I
6	KCM141121	4.0	KNOBE-D12 UL-I
7	21302-5613	1.0	PANEL & KEY BOARD See Fig [H7]
1 to 7	21302-5679	1.0	LTxx2 FRONT PANEL(2CH) See Fig [H6]

I. Removal of the Rear Panel Assembly

Remove the upper and bottom covers.

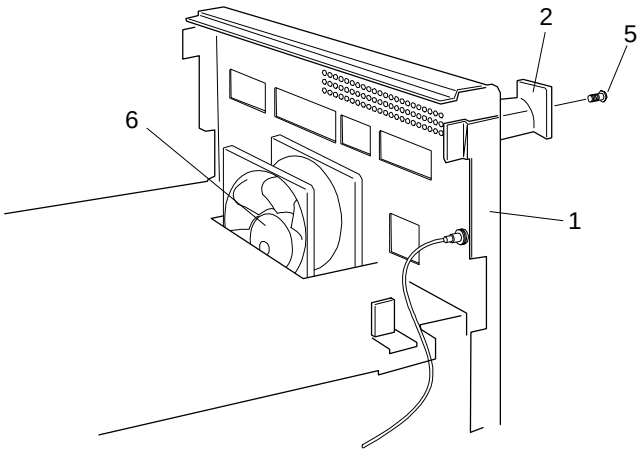
Remove the processor assembly.

Remove the main assembly.

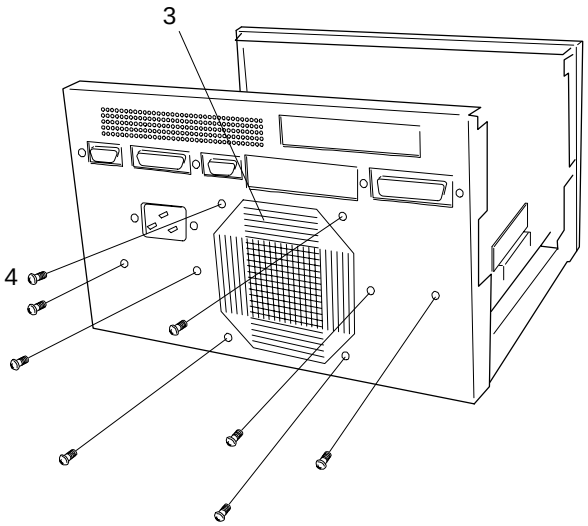
Remove the power supply assembly.

- I1 : Remove the rear panel assembly and four M3 x 6 screws from the main frame.
- I2 : Remove four fan motor fastening M3 x 6 screws.

[I1]



[I2]



Rear Panel Replaceable Parts

Item	IWATSU Part Number	Quantity	Description
1	KBA785111	1.0	REAR FRAME
2	KCM138221	4.0	Cord rack 78 UL-I
3	KSN091911	1.0	WIRE NET(MESH #5)
4	MKB130062	8.0	Screw M3x6
5	MSM140101	4.0	Screw SM1-4X10
6	DMT620701	1.0	FAN 109R1212M114

Assembly Note :

- **Fan** : Check the fan cable direction. Note the air flow, the fan extracts air from the unit and expels it.

- **Feet** : Check that the lower feet and rear cord rack are aligned and properly tightened before re-assembly.

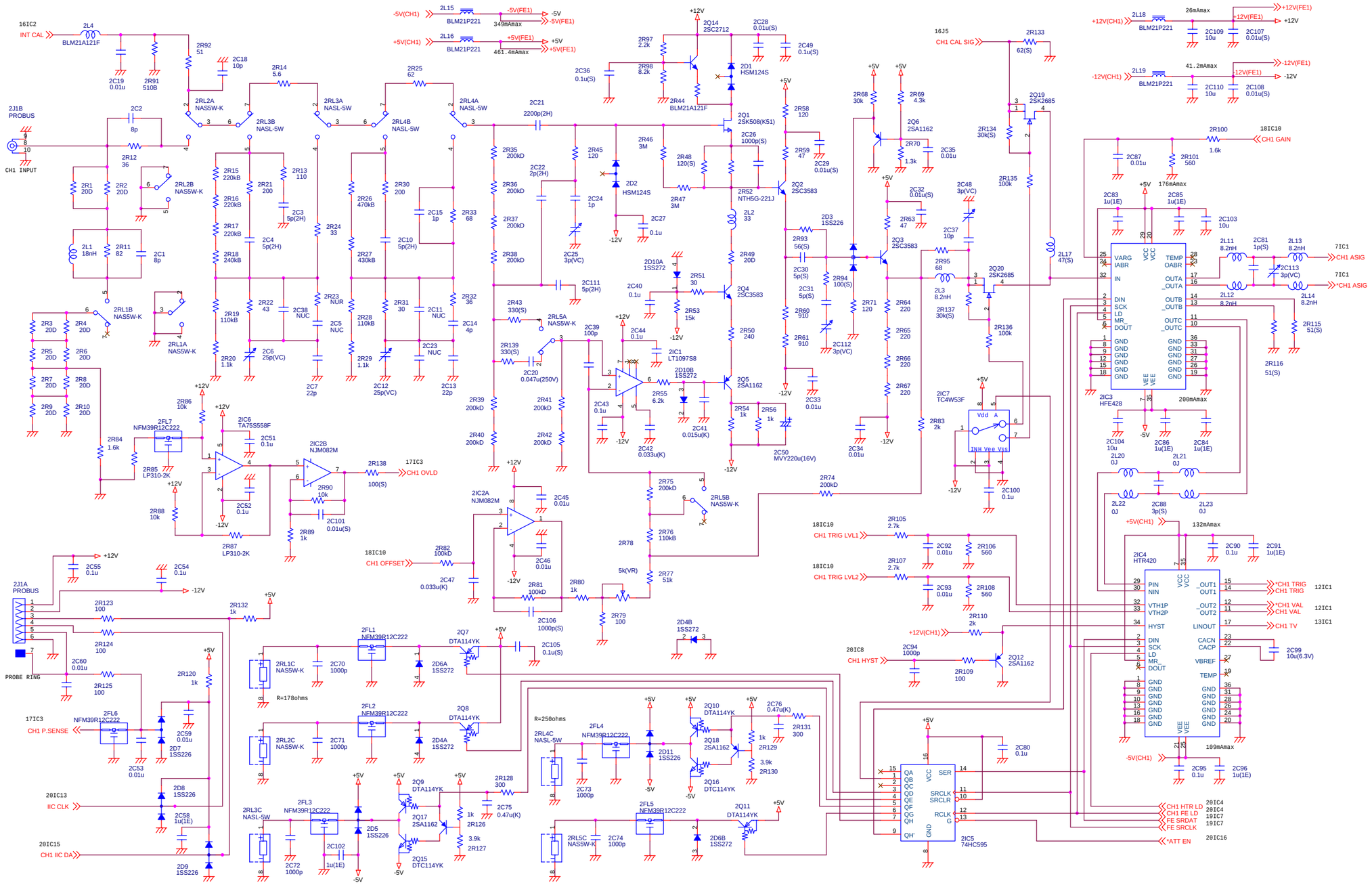
- **Floppy** : Adjust the floppy position to obtain the front face tangential to face of the front panel. Check that the door is moving freely and shuts correctly.
  Insert a floppy and eject it to check the mechanism.

- **Front Panel** : Check that knobs rotate freely, are the right size and in the right place. Do not forget the gasket, see Fig [H6].

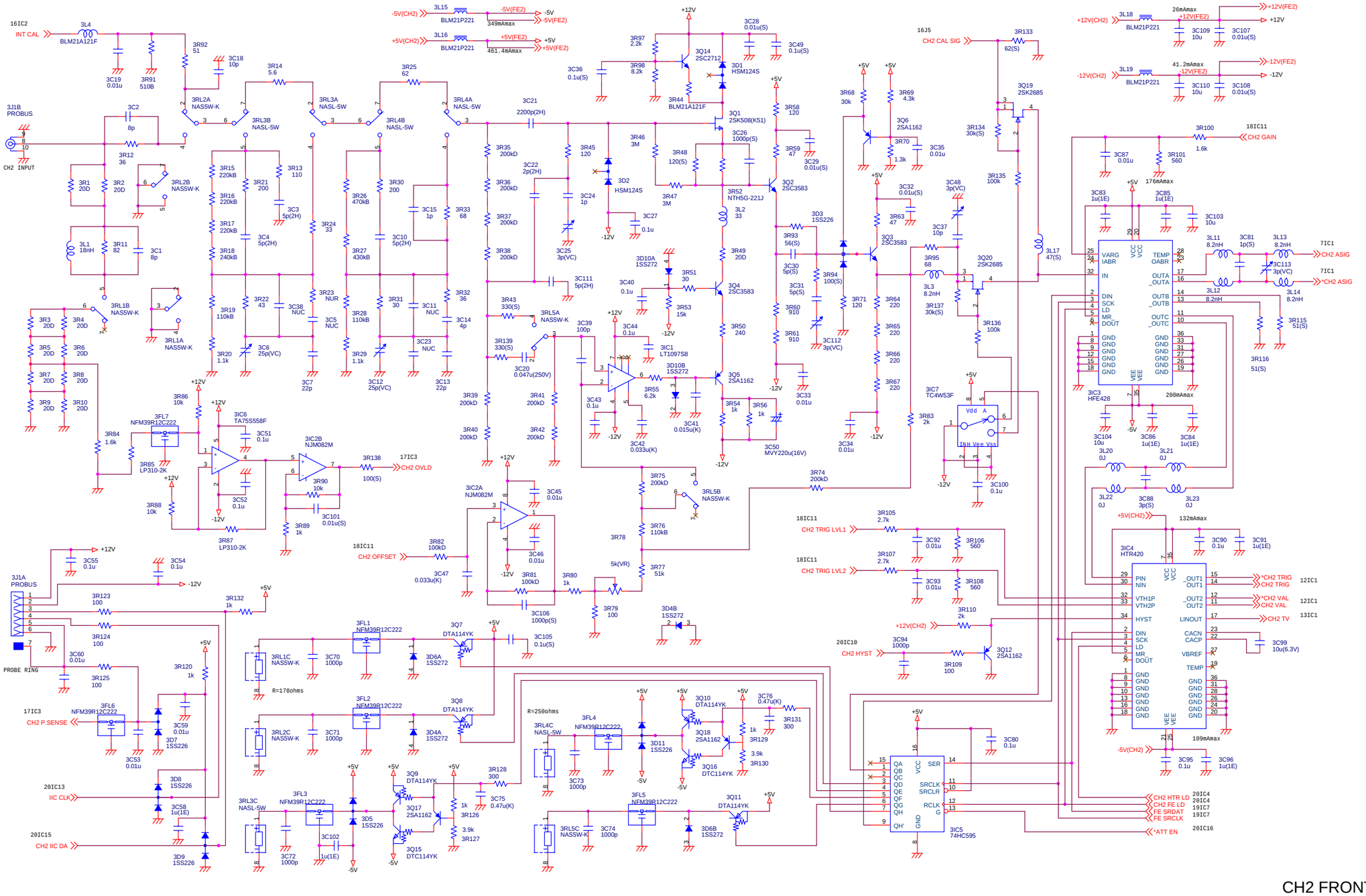
- **Main Board** :The main card must be parallel and tacked against the bend of the lower cover. Being careful not to bend the board or damage components underneath.

- **Processor** : Check that the memory card insertion guide is correctly inserted in the front panel.

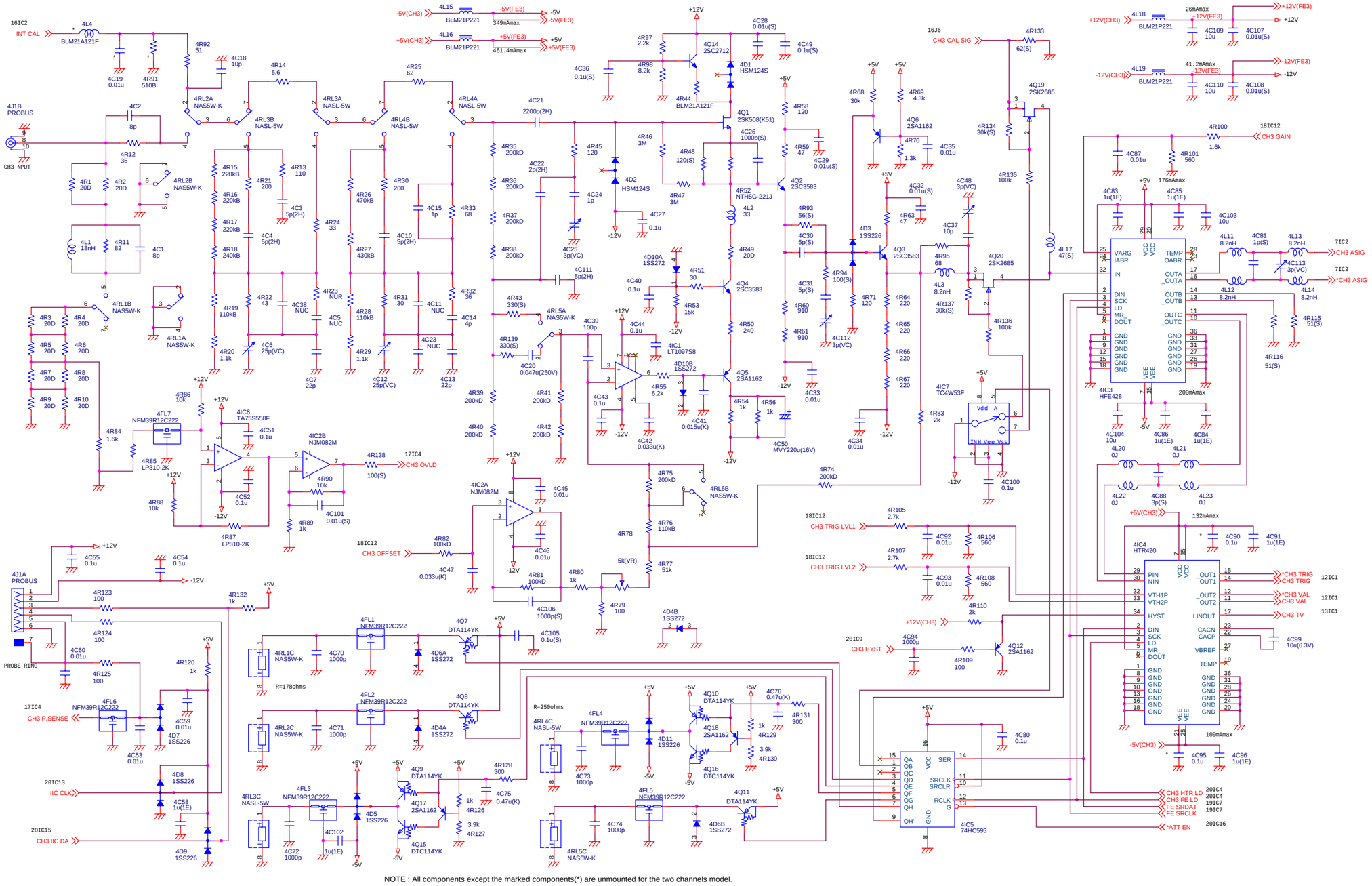
- **Printer** : If the graphic printer is used, before closing don't forget to plug input cable to the option and the driver cable to the processor card.



CH1 FRONT END (2)

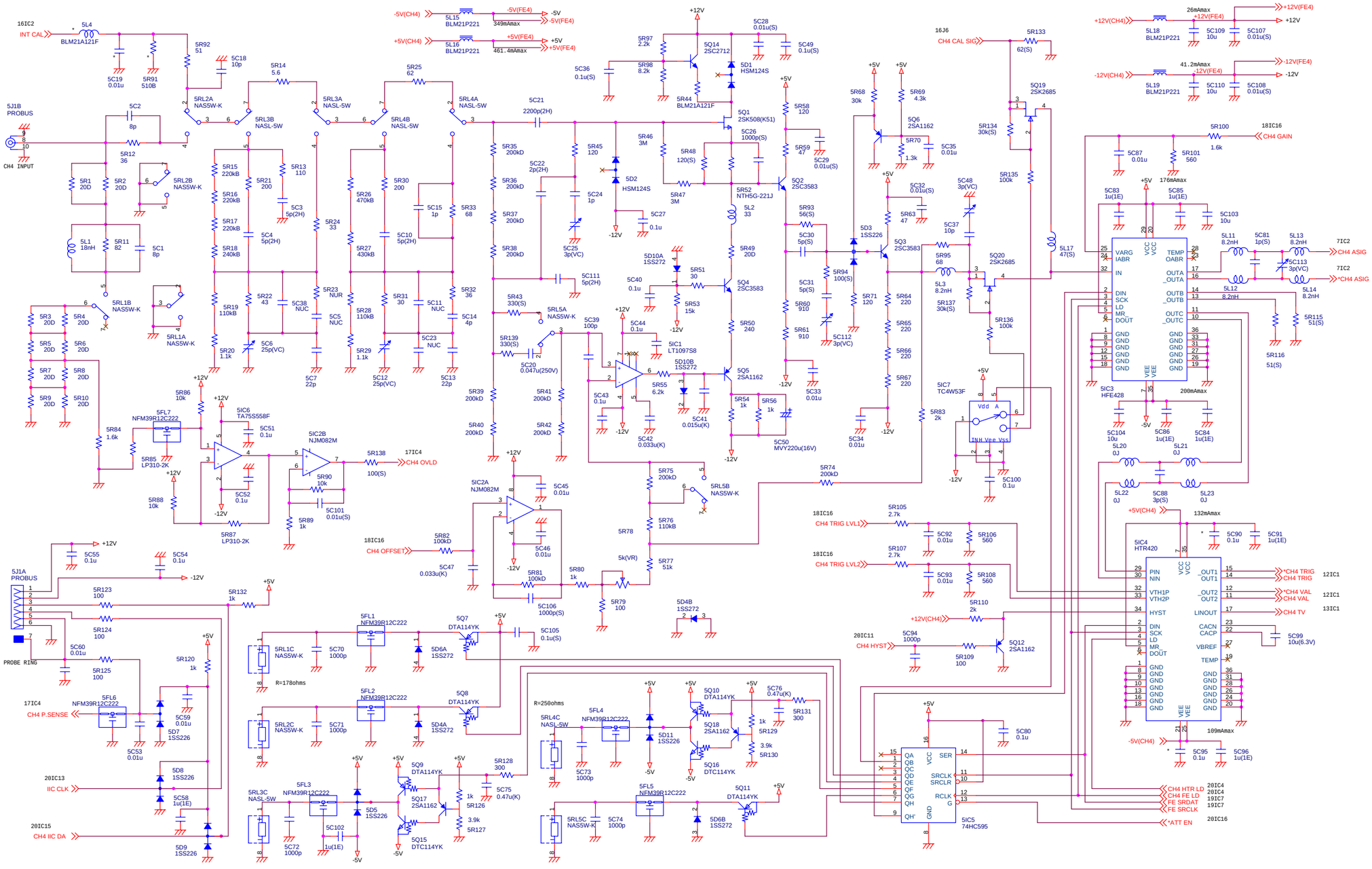


CH2 FRONT END (3)



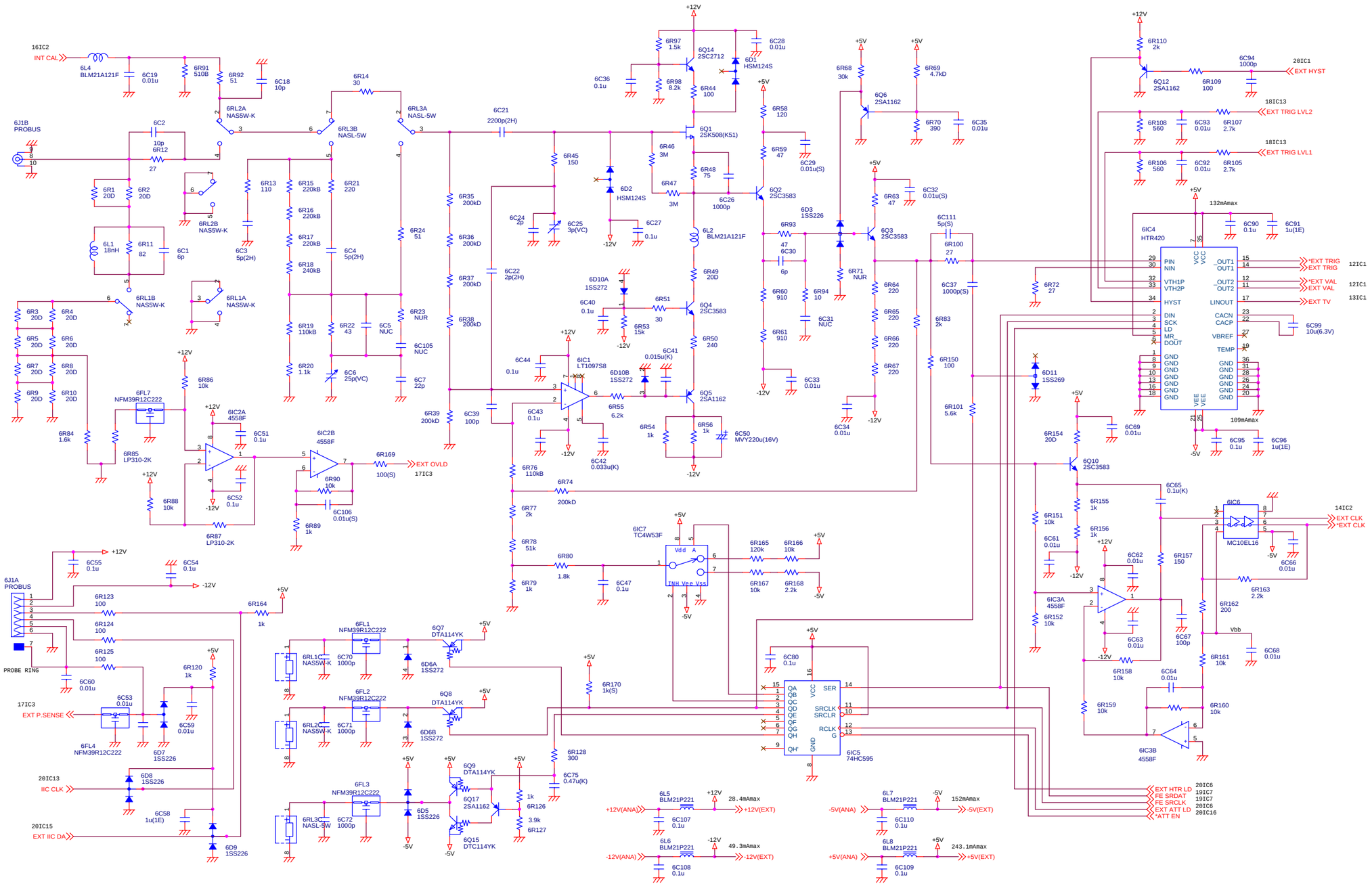
NOTE : All components except the marked components(*) are unmounted for the two channels model.

CH3 FRONT END (4)

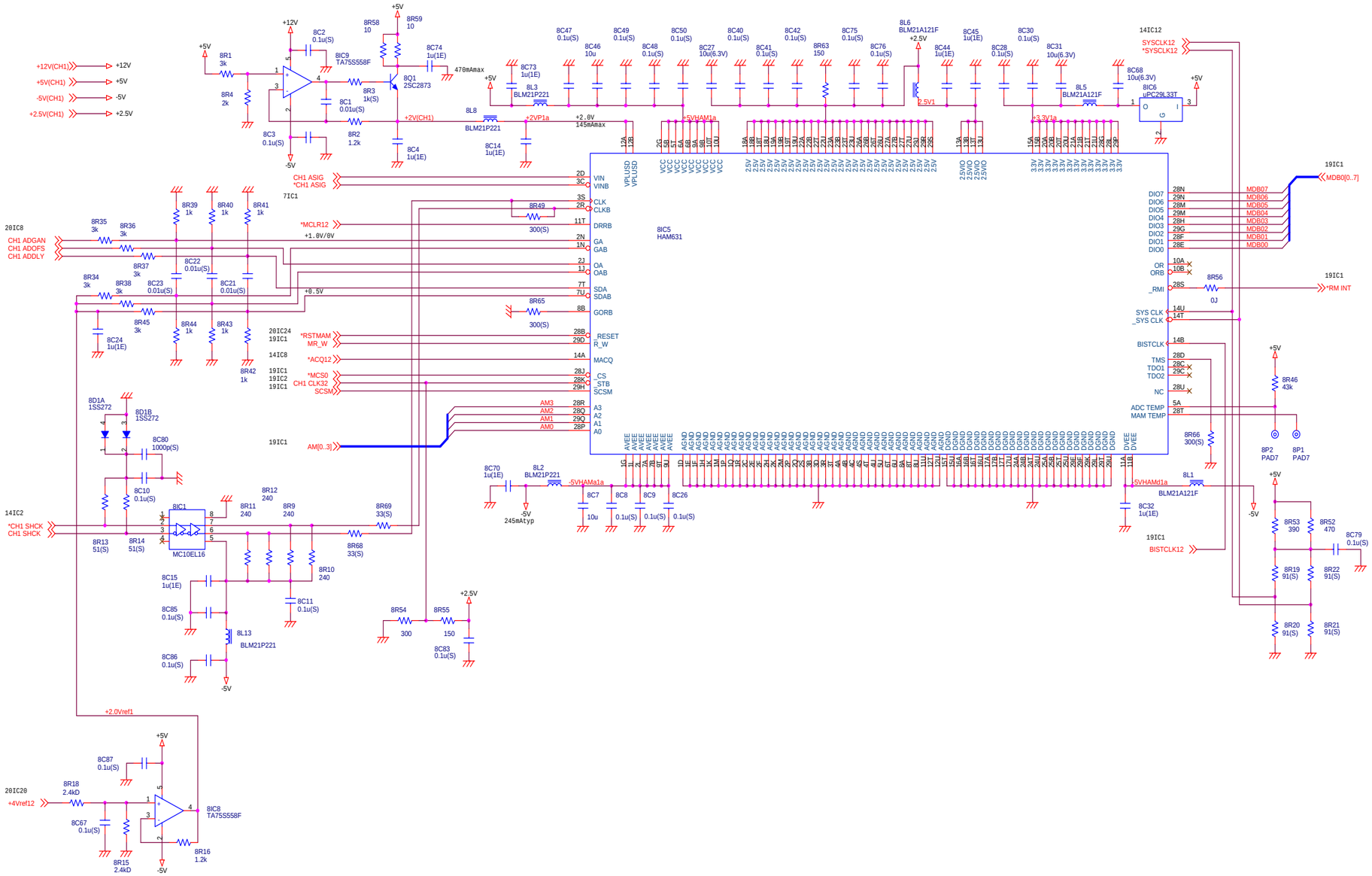


NOTE : All components except the marked components(*) are unmounted for the two channels model.

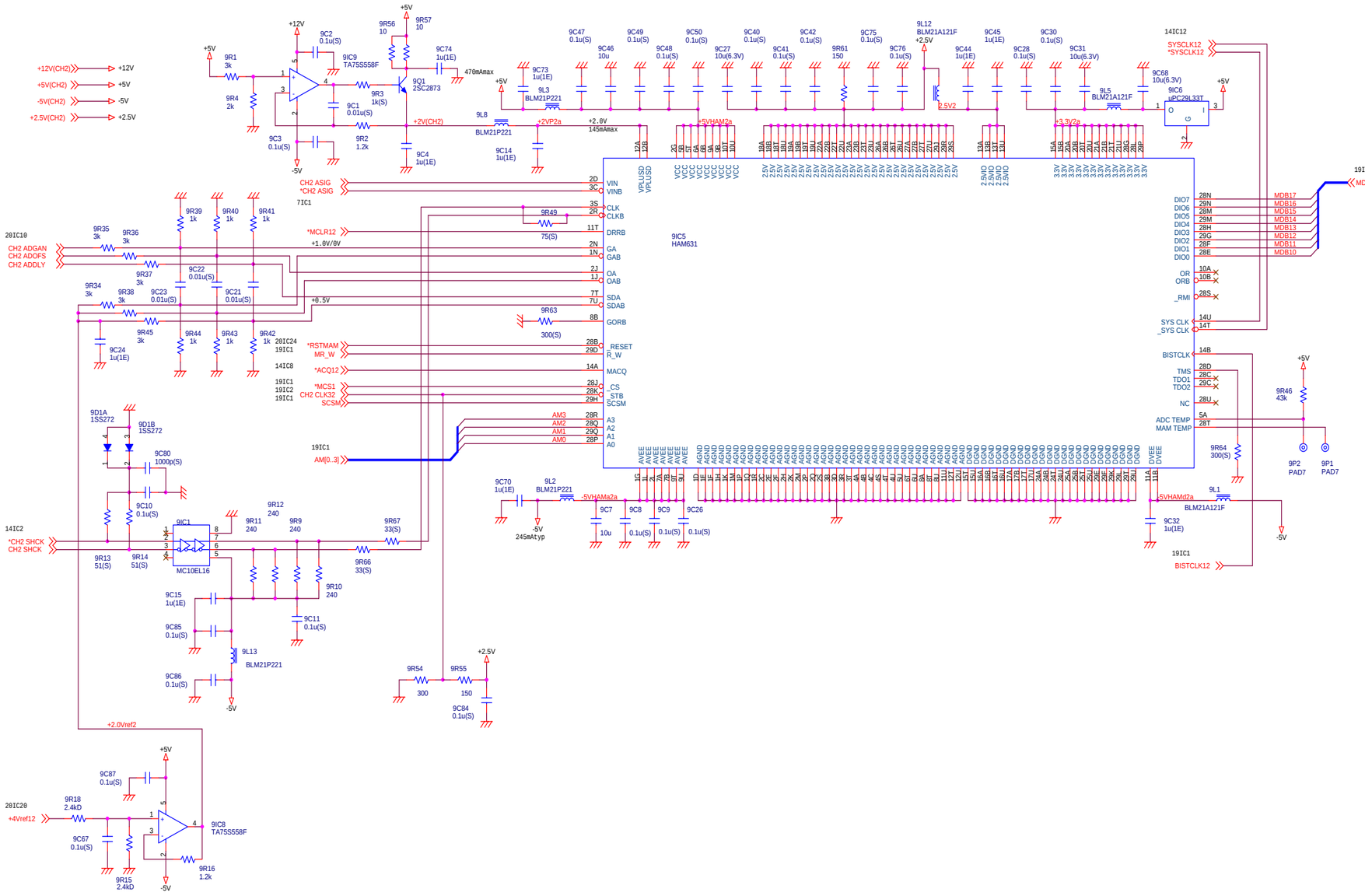
CH4 FRONT END (5)



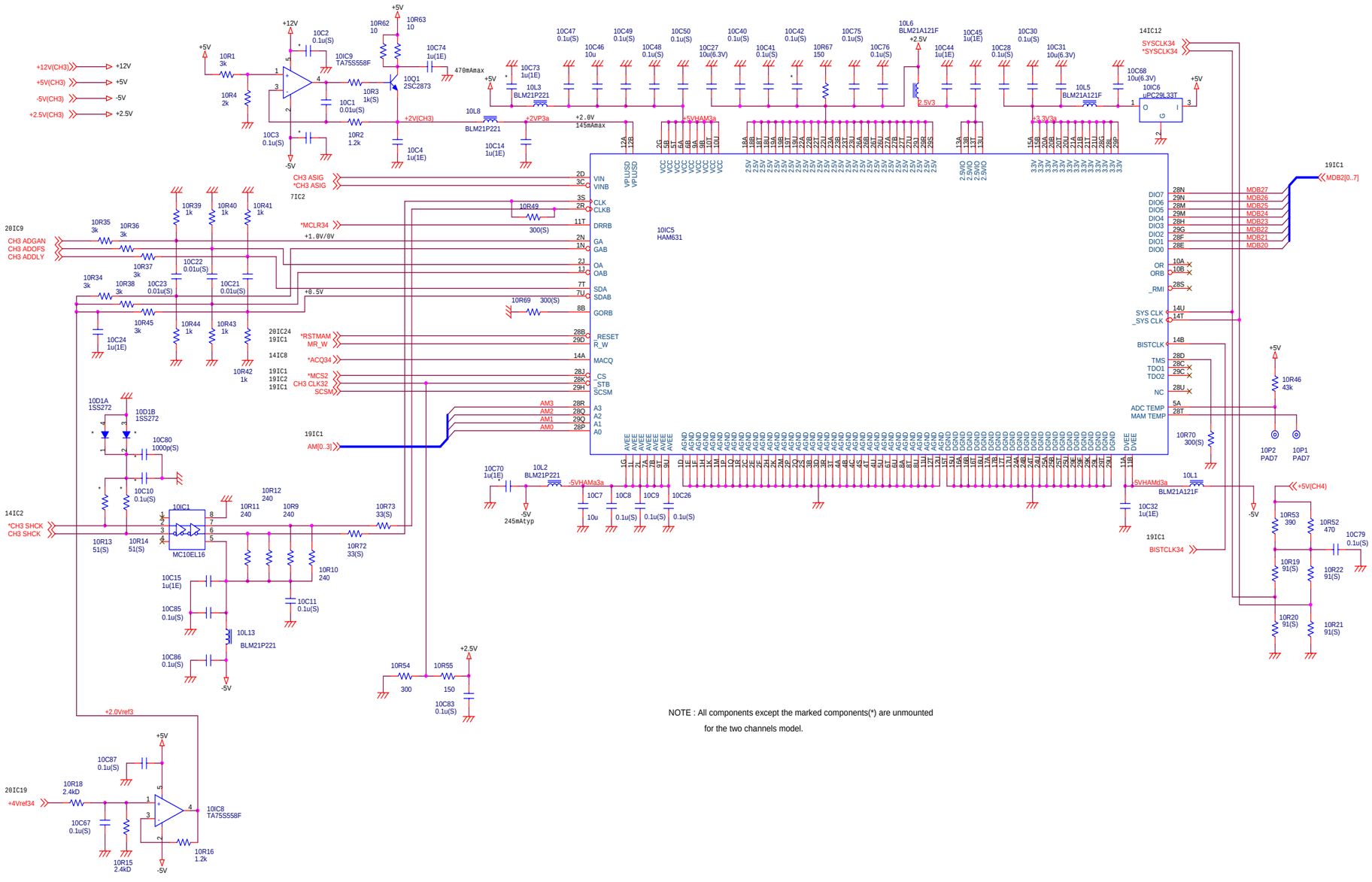
EXT TRIGGER (6)


+12V(CH1)
+5V(CH1)
-5V(CH1)
+2.5V(CH1)
+12V
+5V
-5V
+2.5V
8R1 3k
8R4 2k
8C1 0.01u(S)
8C2 0.1u(S)
8C3 0.1u(S)
8C4 1u(1E)
8C9 TA75S558F
8R2 1.2k
8R3 1k(S)
8Q1 2SC2873
8R58 10
8R59 10
8C74 1u(1E)
470mAmax
+2V(CH1)
8L8 BLM21P221
+2VP1a
+2.0V 145mAmax
8C14 1u(1E)
8L3 BLM21P221
8C73 1u(1E)
8C47 0.1u(S)
8C46 10u
8C49 0.1u(S)
8C48 0.1u(S)
8C50 0.1u(S)
8C27 10u(6.3V)
8C40 0.1u(S)
8C41 0.1u(S)
8C42 0.1u(S)
8R63 150
8C75 0.1u(S)
8C76 0.1u(S)
8L6 BLM21A121F
+2.5V
2.5V1
8C44 1u(1E)
8C45 1u(1E)
8C28 0.1u(S)
8C30 0.1u(S)
8C31 10u(6.3V)
8L5 BLM21A121F
+3.3V1a
8C68 10u(6.3V)
8IC6 uPC29L33T
14IC12
SYSCLK12
*SYSCLK12
+5VHAM1a
8IC5 HAM631
CH1 ASIG
*CH1 ASIG
7IC1
*MCLR12
+1.0V/0V
+0.5V
*RSTMAM
MR_W
*ACQ12
*MCS0
CH1 CLK32
SCSM
AM[0..3]
19IC1
20IC8
CH1 ADGAN
CH1 ADOFS
CH1 ADDLY
8R35 3k
8R36 3k
8R37 3k
8R34 3k
8R38 3k
8R45 3k
8R39 1k
8R40 1k
8R41 1k
8R44 1k
8R43 1k
8R42 1k
8C22 0.01u(S)
8C21 0.01u(S)
8C23 0.01u(S)
8C24 1u(1E)
8R49 300(S)
8R65 300(S)
8D1A 1SS272
8D1B 1SS272
8C80 1000p(S)
8C10 0.1u(S)
14IC2
*CH1 SHCK
CH1 SHCK
8R13 51(S)
8R14 51(S)
8IC1
MC10EL16
8R12 240
8R11 240
8R9 240
8R10 240
8R69 33(S)
8R68 33(S)
8C15 1u(1E)
8C85 0.1u(S)
8C86 0.1u(S)
8C11 0.1u(S)
8L13 BLM21P221
8R54 300
8R55 150
8C83 0.1u(S)
+2.5V
+2.0Vref1
20IC20
+4Vref12
8R18 2.4kΩ
8R15 2.4kΩ
8C67 0.1u(S)
8C87 0.1u(S)
8IC8 TA75S558F
8R16 1.2k
8C70 1u(1E)
8L2 BLM21P221
-5VHAMa1a
-5V 245mAtyp
8C7 10u
8C8 0.1u(S)
8C9 0.1u(S)
8C26 0.1u(S)
8C32 1u(1E)
8L1 BLM21A121F
-5VHAMd1a
19IC1
BISTCLK12
MDB[0..7]
MDB07
MDB06
MDB05
MDB04
MDB03
MDB02
MDB01
MDB00
*RM INT
8R56 0J
SYS CLK
_SYS CLK
BISTCLK
TMS
TDO1
TDO2
NC
ADC TEMP
MAM TEMP
8R66 300(S)
8R46 43k
8P2 PAD7
8P1 PAD7
8R53 390
8R52 470
8C79 0.1u(S)
8R19 91(S)
8R22 91(S)
8R20 91(S)
8R21 91(S)

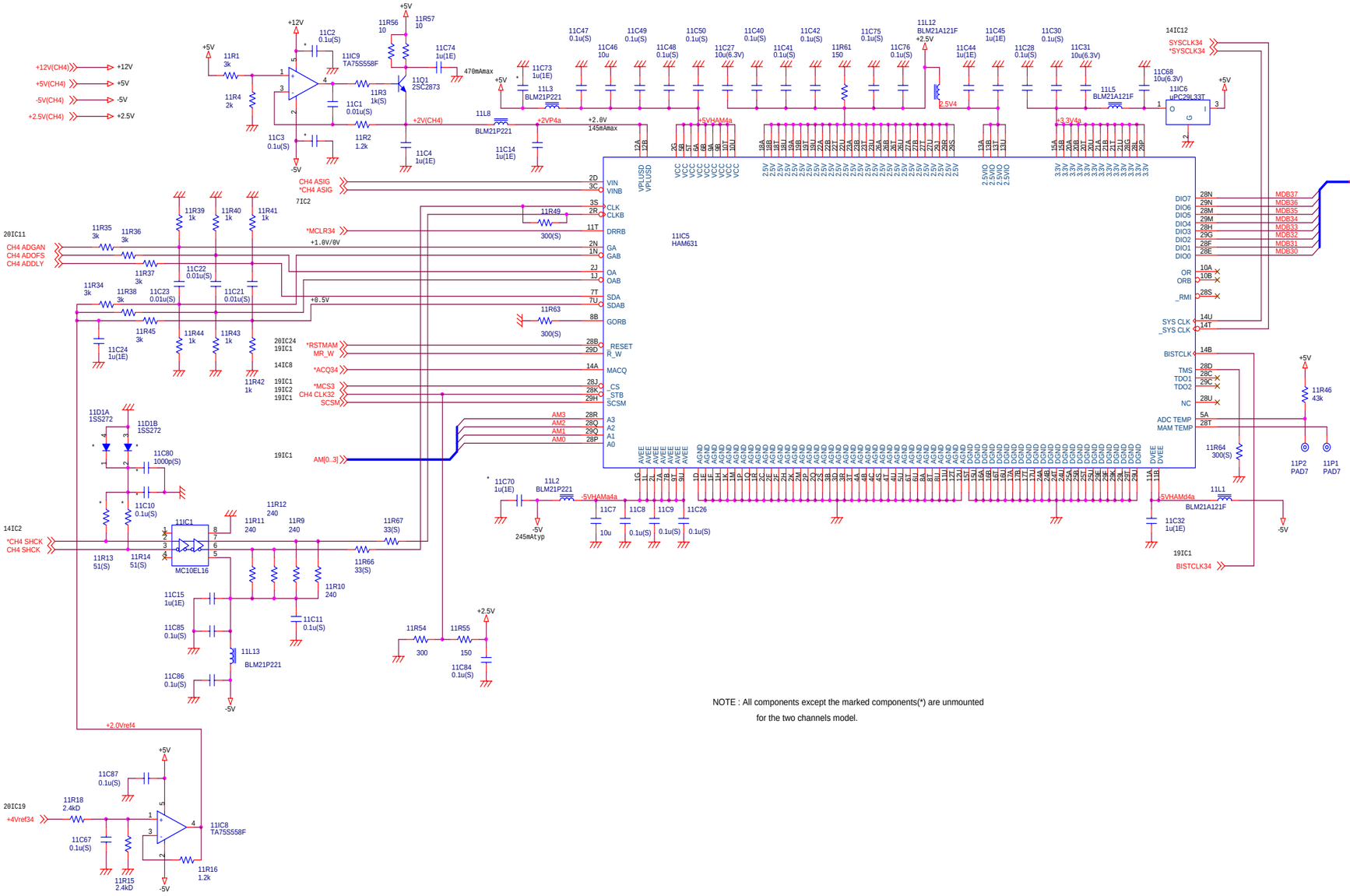
CH1 A/D CNVT (8)


+12V(CH2)
+5V(CH2)
-5V(CH2)
+2.5V(CH2)
CH2 ASIG
*CH2 ASIG
CH2 ADGAN
CH2 ADOFS
CH2 ADDLY
*MCLR12
*RSTMAM
MR_W
*ACQ12
*MCS1
CH2 CLK32
SCSM
AM[0..3]
*CH2 SHCK
CH2 SHCK
+2.0Vref2
+4Vref12
+2V(CH2)
+2VP2a
+5VHAM2a
-5VHAMa2a
-5VHAMd2a
+3.3V2a
+2.5V2
SYSCLK12
*SYSCLK12
BISTCLK12
MDB[0..7]
9IC5
HAM631
9IC1
9IC2
9IC8
TA75S558F
MC10EL16
BLM21P221
BLM21A121F
uPC29L33T
245mAtyp
47.0mAmax
145mAmax
7IC1
14IC12
20IC10
20IC20
14IC2
19IC1
14IC8

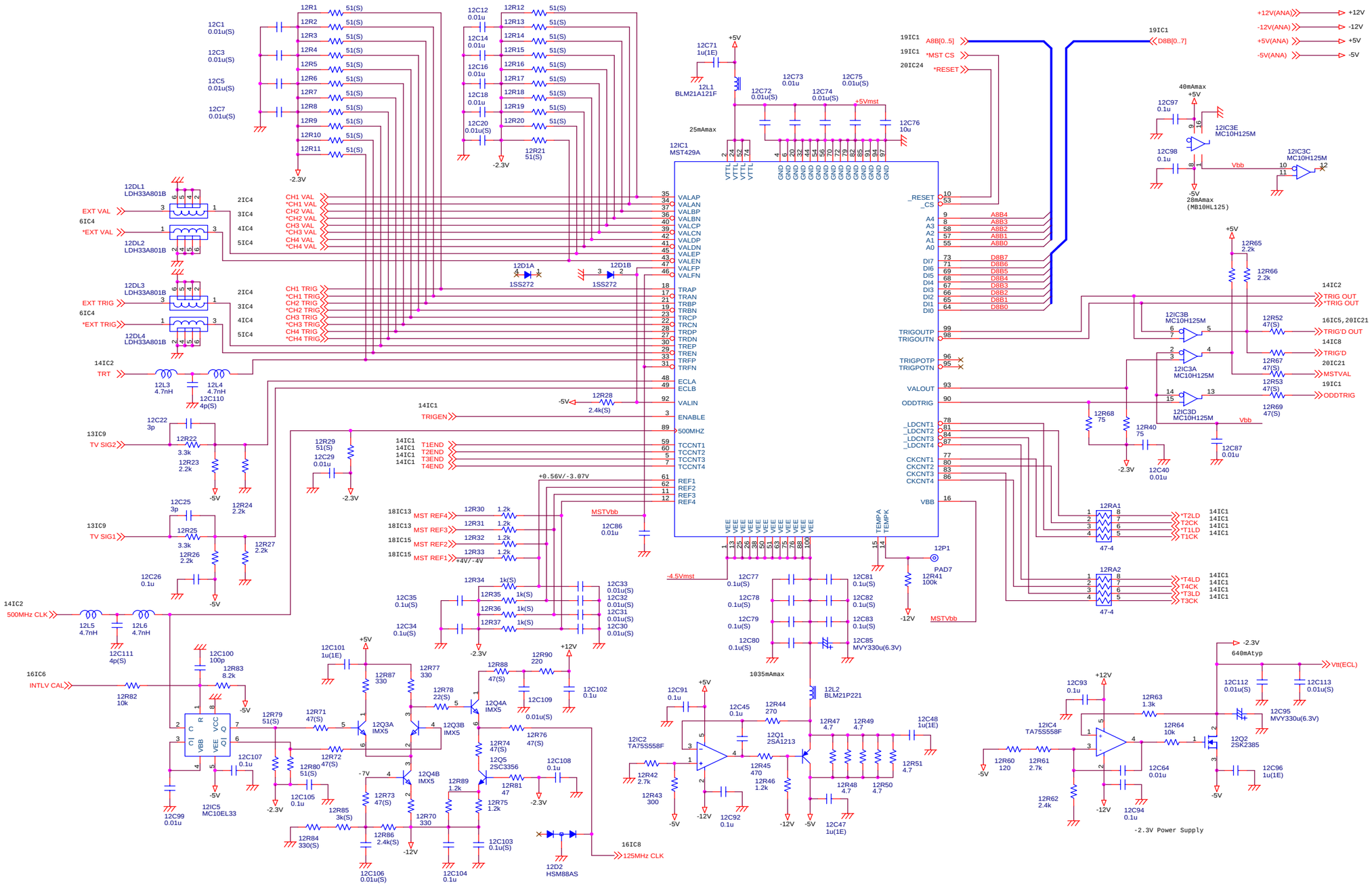
CH2 A/D CNVT (9)

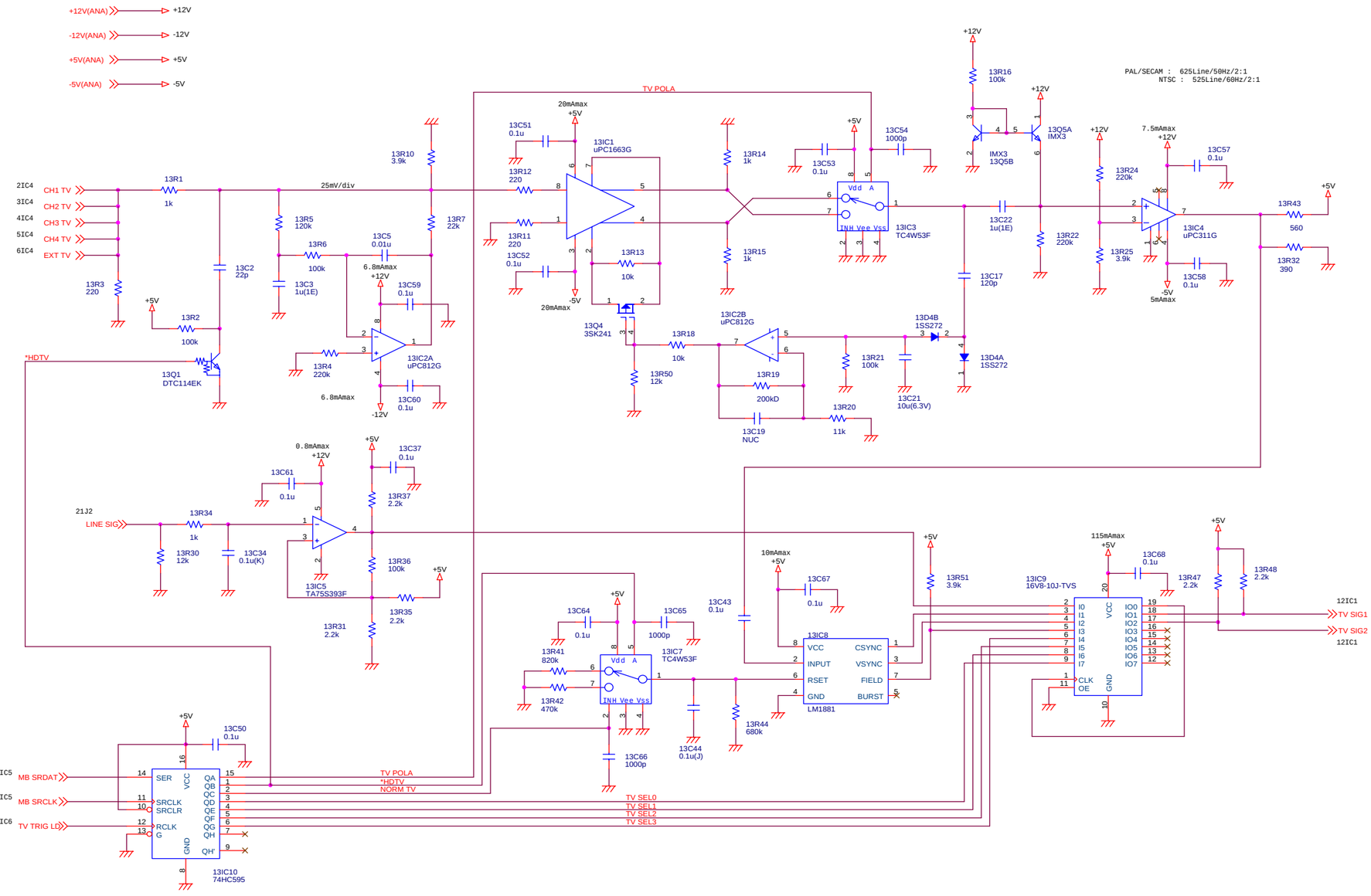


CH3 A/D CNVT (10)

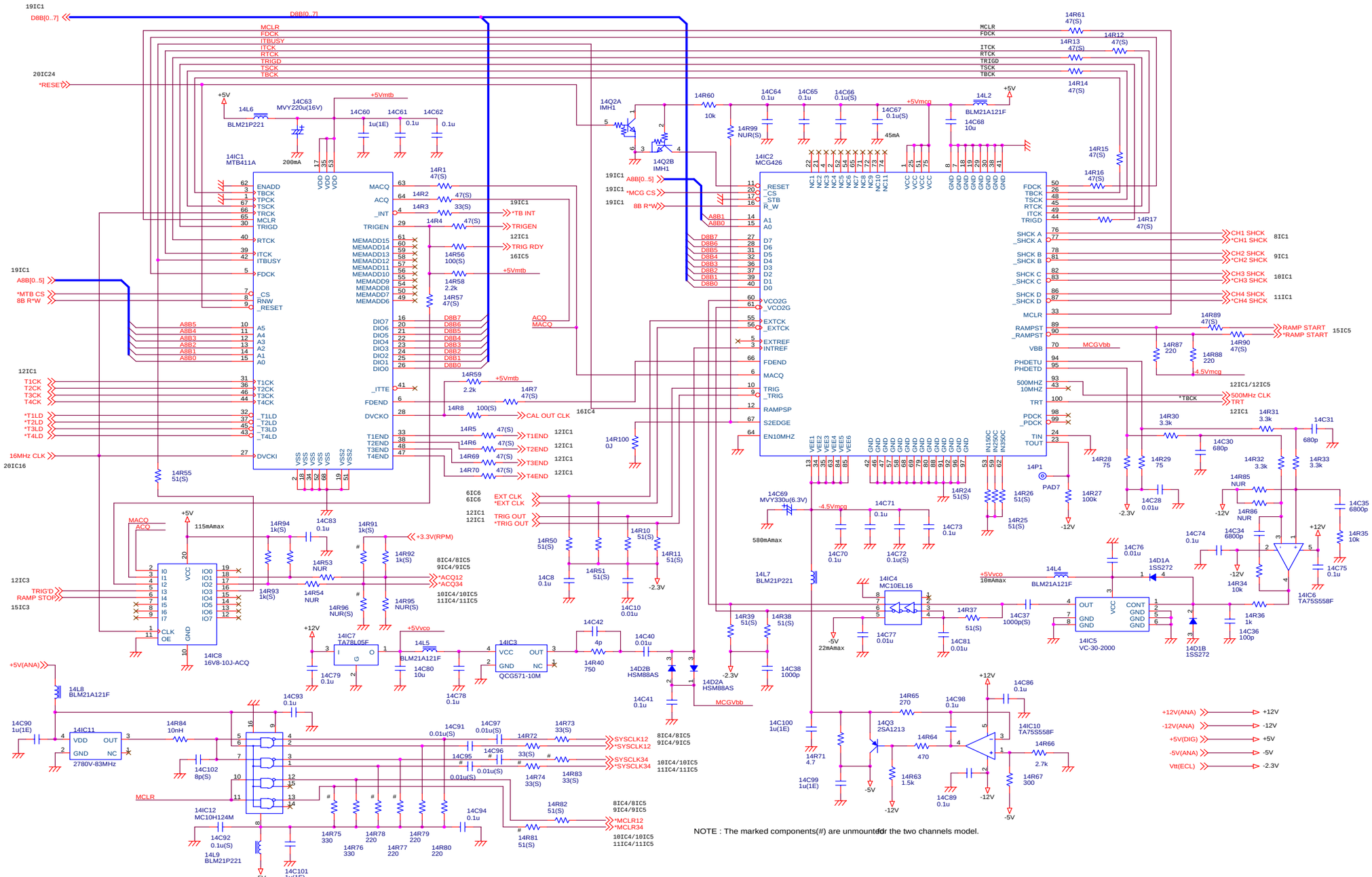


CH4 A/D CNVT (11)


TRIGGER (12)

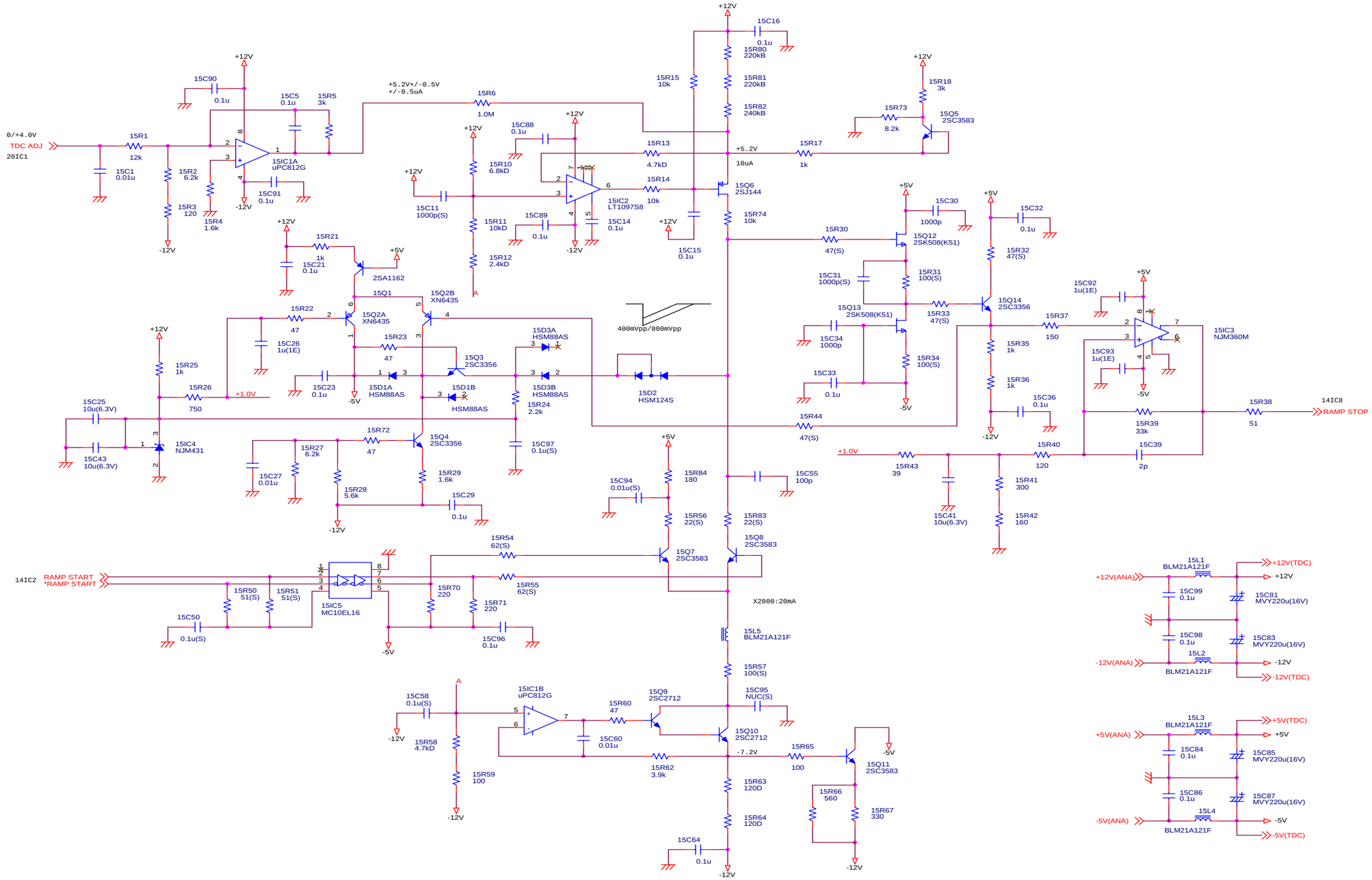


TV SYNC SEP (13)

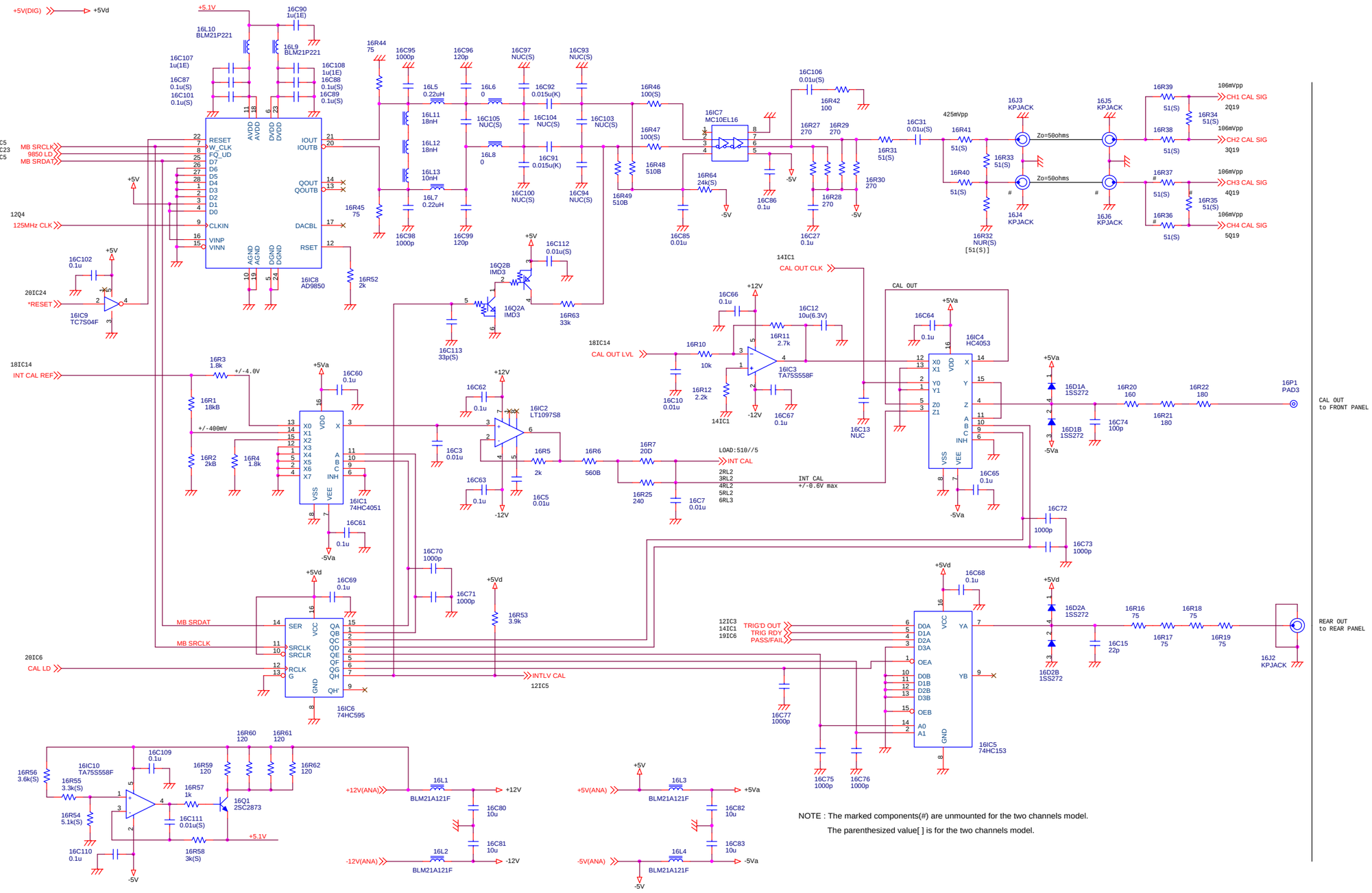


NOTE : The marked components(#) are unmounted for the two channels model.

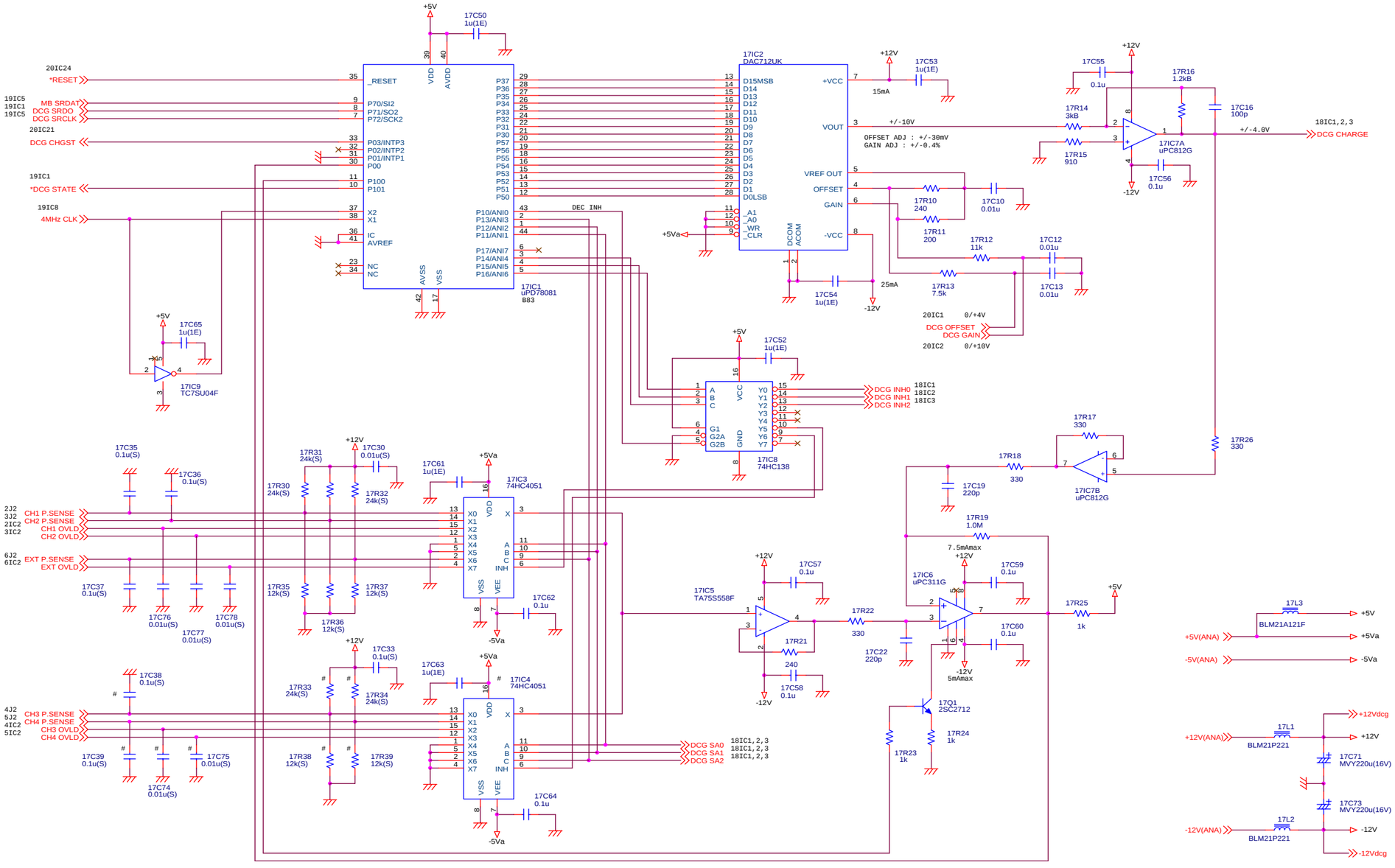
TIMEBASE (14)


0/+4.0V
TDC ADJ
20IC1
15R1 12k
15C1 0.01u
15R2 6.2k
15R3 120
15R4 1.6k
15IC1A uPC812G
15C90 0.1u
15C5 0.1u
15R5 3k
15C91 0.1u
+5.2V+/-0.5V
+/-0.5uA
15R6 1.0M
15C88 0.1u
15R10 6.8kD
15R11 10kD
15R12 2.4kD
15C89 0.1u
15C14 0.1u
15IC2 LT1097S8
15R13 4.7kD
15R14 10k
15C11 1000p(S)
15C15 0.1u
15R15 10k
15C16 0.1u
15R80 220kB
15R81 220kB
15R82 240kB
+5.2V
10uA
15Q6 2SJ144
15R74 10k
15R17 1k
15R18 3k
15R73 8.2k
15Q5 2SC3583
15R21 1k
15C21 0.1u
2SA1162
15Q1
15Q2A XN6435
15Q2B XN6435
15R22 47
15C26 1u(1E)
15R23 47
15C23 0.1u
15D1A HSM88AS
15D1B HSM88AS
15Q3 2SC3356
15D3A HSM88AS
15D3B HSM88AS
15R24 2.2k
15D2 HSM124S
400mVpp/800mVpp
15R25 1k
15R26 750
+1.0V
15C25 10u(6.3V)
15C43 10u(6.3V)
15IC4 NJM431
15R72 47
15R27 6.2k
15C27 0.01u
15R28 5.6k
15Q4 2SC3356
15R29 1.6k
15C29 0.1u
15C97 0.1u(S)
15R30 47(S)
15Q12 2SK508(K51)
15C30 1000p
15C31 1000p(S)
15R31 100(S)
15Q13 2SK508(K51)
15C34 1000p
15C33 0.1u
15R33 47(S)
15R34 100(S)
15Q14 2SC3356
15R32 47(S)
15C32 0.1u
15R35 1k
15R36 1k
15C36 0.1u
15R37 150
15R44 47(S)
15C92 1u(1E)
15C93 1u(1E)
15IC3 NJM360M
15R39 33k
15R38 51
14IC8
RAMP STOP
15R40 120
15C39 2p
15R43 39
15C41 10u(6.3V)
15R41 300
15R42 160
15C94 0.01u(S)
15R84 180
15R56 22(S)
15R83 22(S)
15Q8 2SC3583
15C55 100p
15Q7 2SC3583
15R54 62(S)
15R55 62(S)
14IC2
RAMP START
*RAMP START
15IC5 MC10EL16
15R50 51(S)
15R51 51(S)
15R70 220
15R71 220
15C50 0.1u(S)
15C96 0.1u
X2000:20mA
15L5 BLM21A121F
15R57 100(S)
15C95 NUC(S)
15C58 0.1u(S)
15IC1B uPC812G
15R58 4.7kD
15R59 100
15R60 47
15C60 0.01u
15Q9 2SC2712
15Q10 2SC2712
-7.2V
15R62 3.9k
15R65 100
15Q11 2SC3583
15R63 120D
15R64 120D
15R66 560
15R67 330
15C64 0.1u
15L1 BLM21A121F
+12V(ANA)
+12V(TDC)
15C99 0.1u
15C81 MVY220u(16V)
15C98 0.1u
15C83 MVY220u(16V)
15L2 BLM21A121F
-12V(ANA)
-12V(TDC)
15L3 BLM21A121F
+5V(ANA)
+5V(TDC)
15C84 0.1u
15C85 MVY220u(16V)
15C86 0.1u
15C87 MVY220u(16V)
15L4 BLM21A121F
-5V(ANA)
-5V(TDC)

T/D CNVT (15)

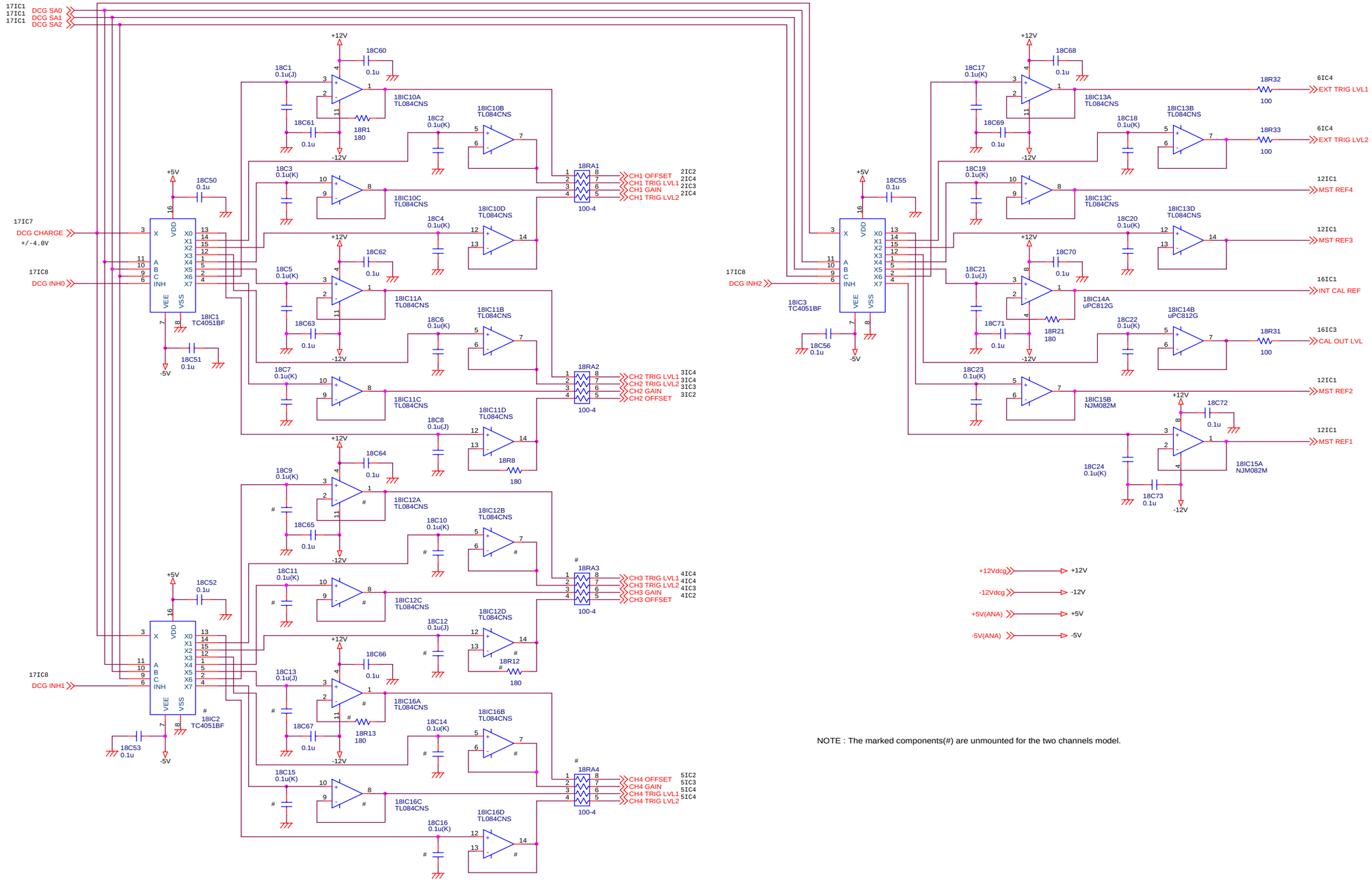


CAL SIGNAL (16)



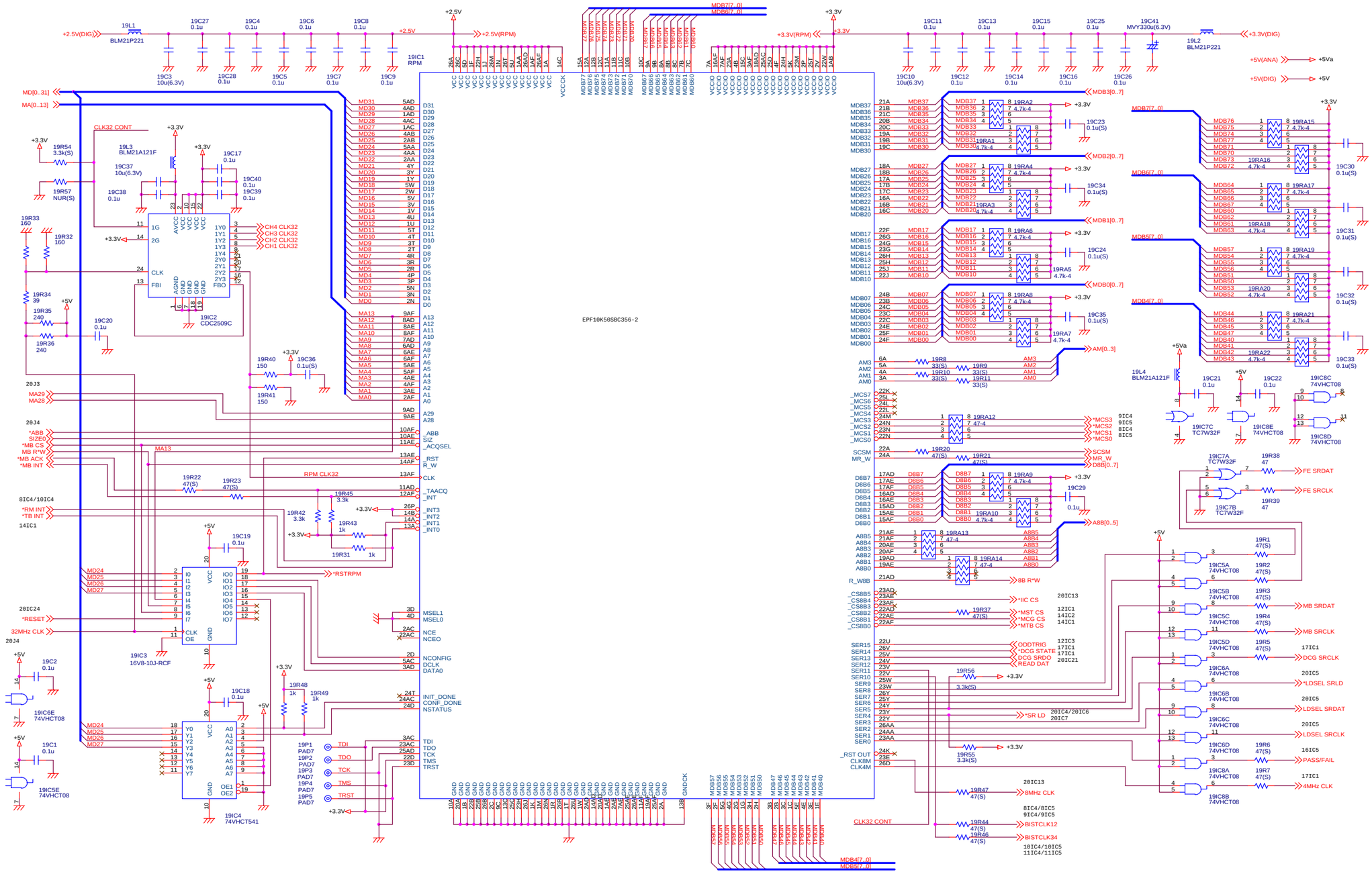
NOTE : The marked components(#) are unmounted for the two channels model.

DC GENE 1/2 (17)

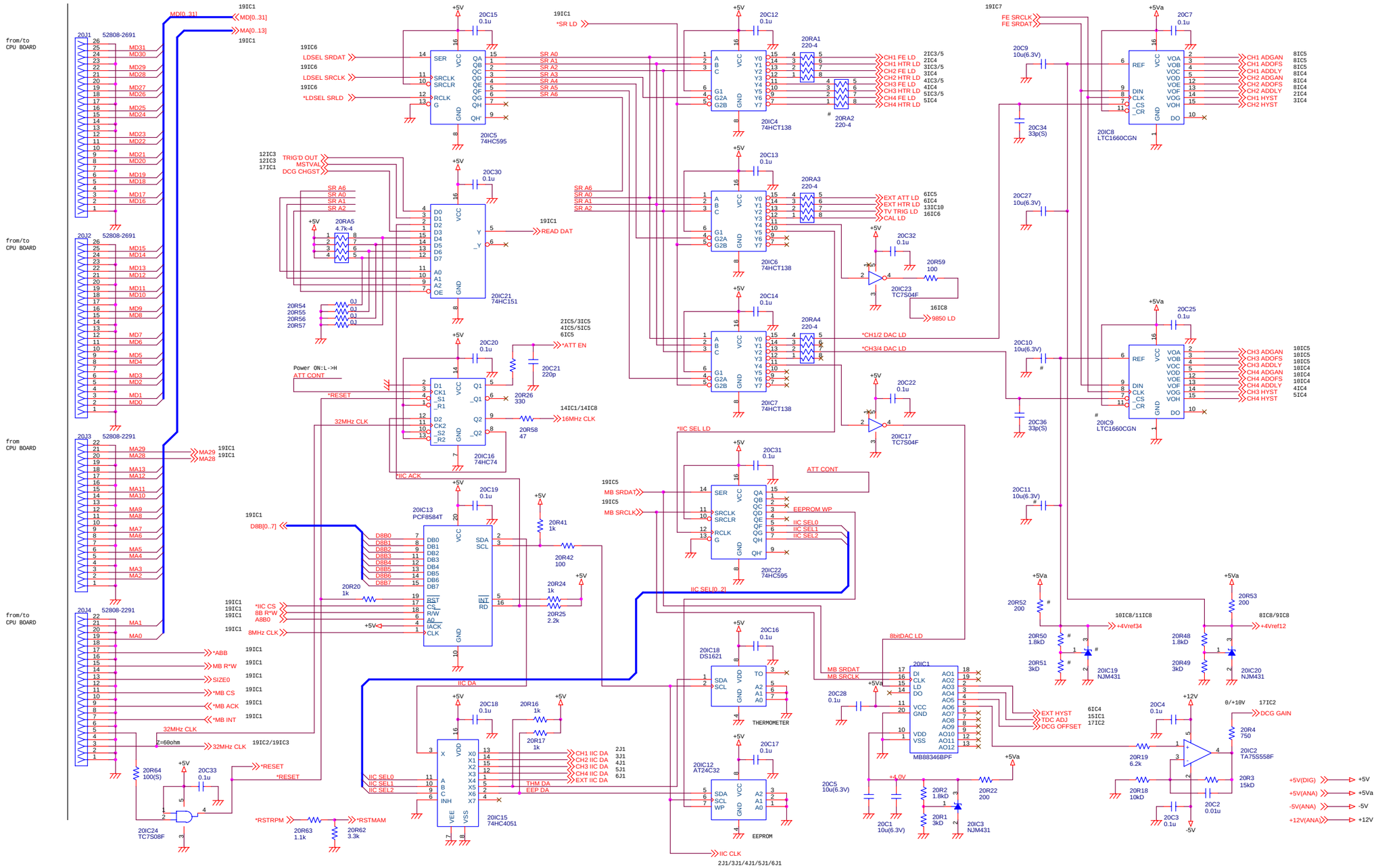


NOTE : The marked components(#) are unmounted for the two channels model.

DC GENE 2/2 (18)

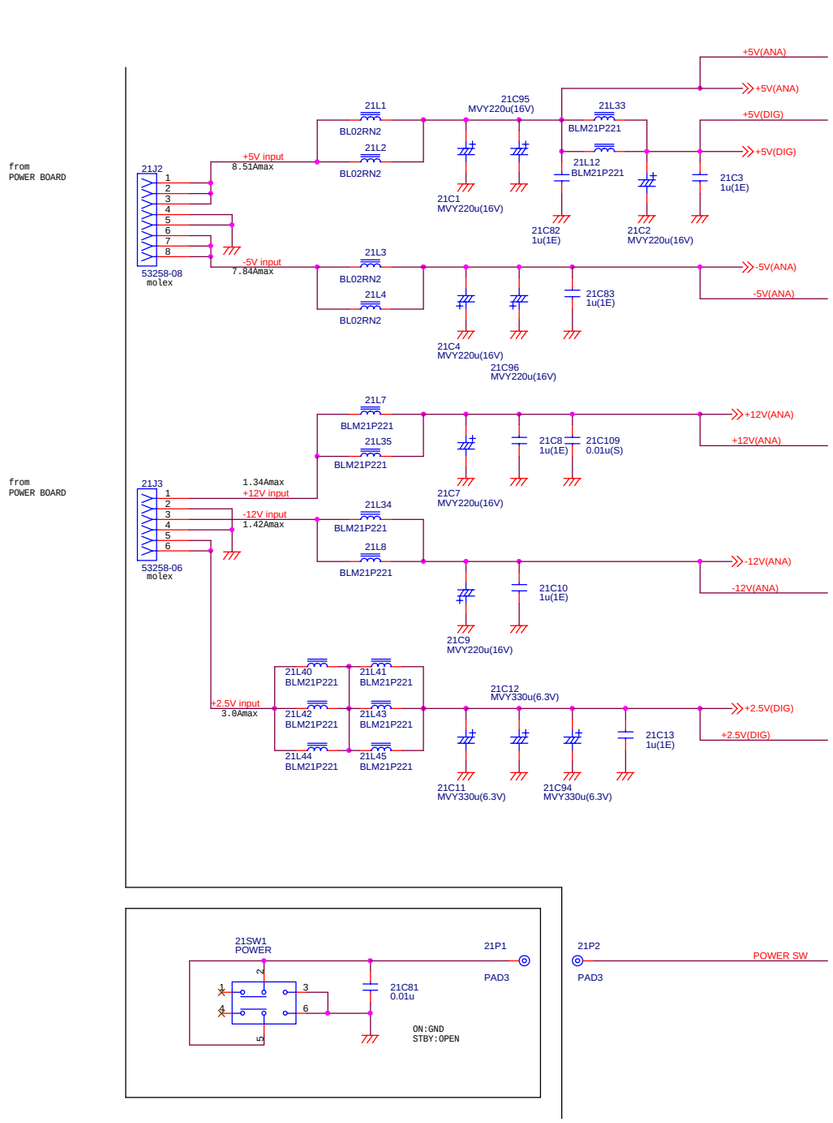


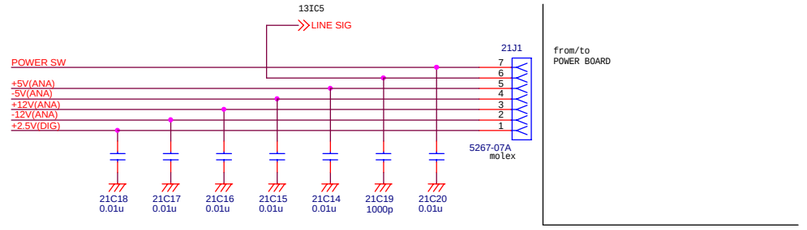
MAIN CONT 1/2 (19)

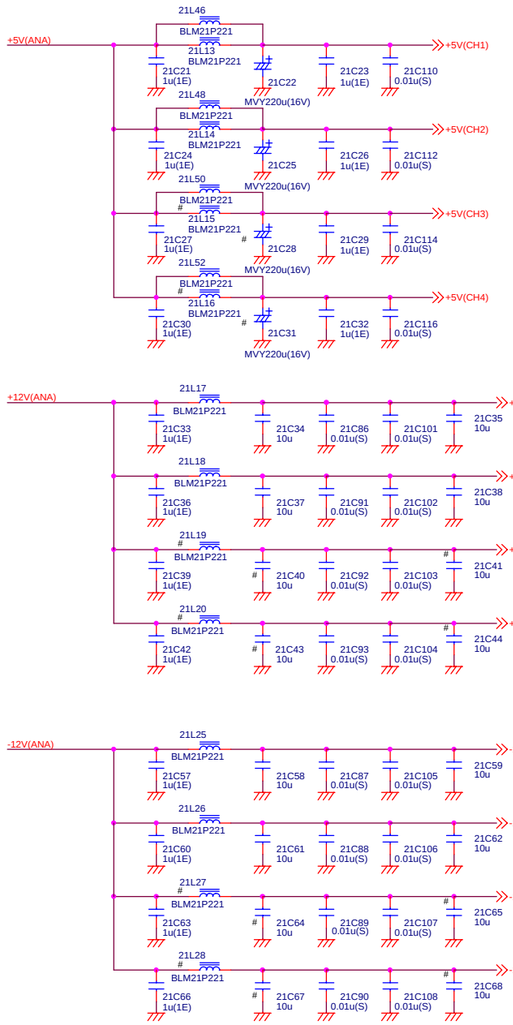


NOTE : The marked components(#) are unmounted for the two channels model.

MAIN CONT 2/2 (20)







NOTE : The marked components(#) are unmounted for the two channels model.

POWER CONNECTOR (21)

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